

Compal Confidential

Model Name : QILE1 & QILE2
File Name : LA-8131P, LA-8133P
BOM P/N:

QILE1:
4319GG39L01 : SMT MB A8131 QILE1 DIS-N13P
4319GG39L02 : SMT MB A8131 QILE1 DIS GPU-N13M
4319GG39L03 : SMT MB A8131 QILE1 UMA

QILE2:
4319GJ39L01 : SMT MB A8133 QILE2 DIS-N13P
4319GJ39L02 : SMT MB A8133 QILE2 DIS GPU-N13M
4319GJ39L03 : SMT MB A8133 QILE2 UMA

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M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH
GPU nVIDIA N13M-GE1 / N13P-GL

2012-01-11

REV:1.0

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Voltage Rails

power plane	State	+B	+5VALW	+3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS	+3VM +1.05VM
S0		○	○	○	○	○	○ M3 Supported
S3		○	○	○	○	✗	○ M3 Supported
S5 S4/AC		○	○	✗	✗	✗	○ M3 Supported
S5 S4/ Battery only		✗	✗	✗	✗	✗	
S5 S4/AC & Battery don't exist		✗	✗	✗	✗	✗	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	0.6
6	
7	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor Fintek F75303M	1001 101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	
		1	USB 3.0 Port (Left Side)
	UHCI1	2	USB 3.0 Port (Left Side)
		3	USB 3.0 Port (Left Side)
	UHCI2	4	
		5	Camera
EHCI2	UHCI3	6	
		7	
	UHCI4	8	
		9	USB Port (Right Side)
	UHCI5	10	Mini Card(WLAN/BT)
		11	FPR
	UHCI6	12	Mini Card(WWAN)
		13	Blue Tooth

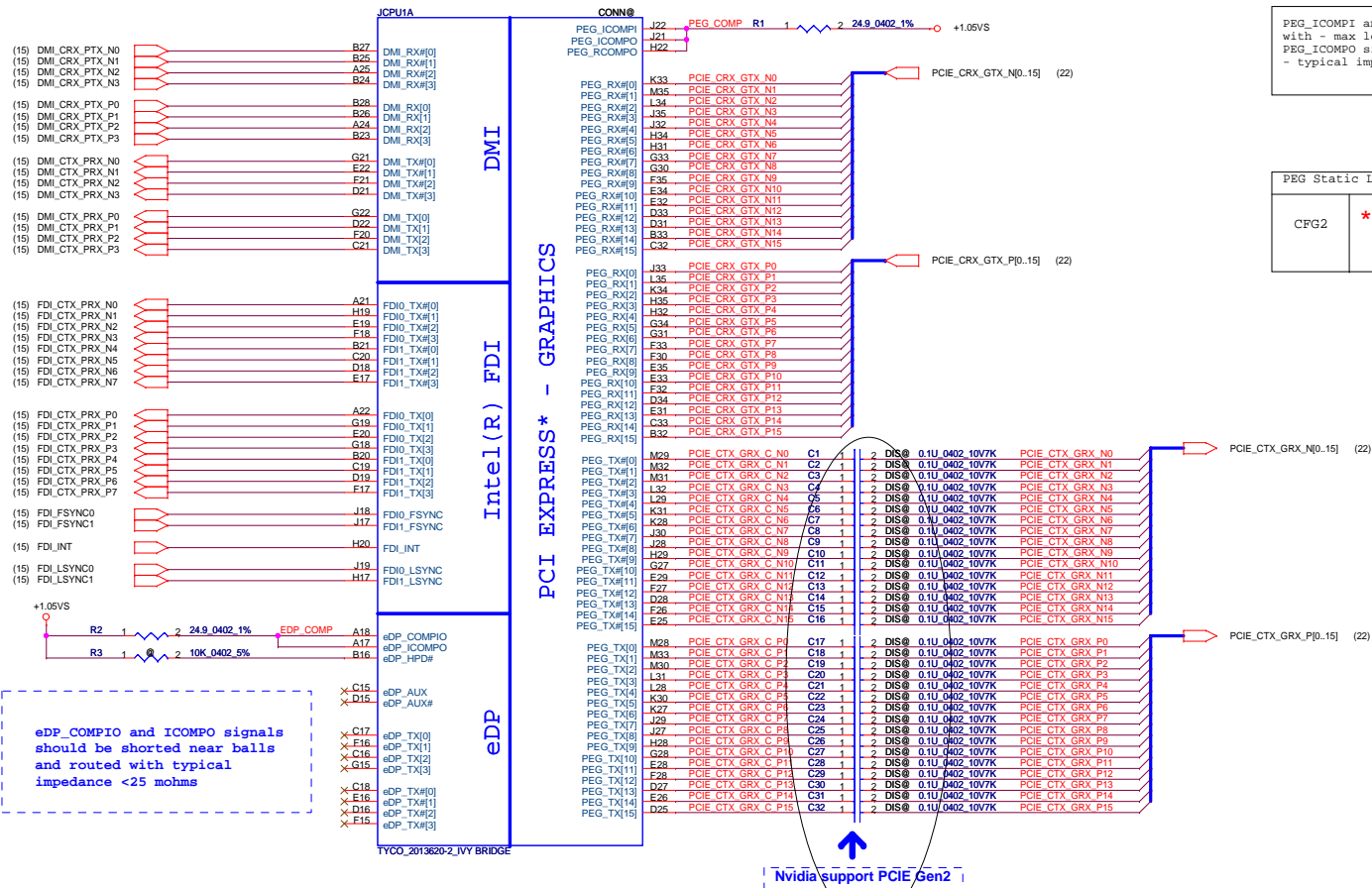
BOM Structure Table

BTO Item	BOM Structure
Connector	CONN@
45 LEVEL	45@
Unpop	@
nVidia	DIS@
INTEL DD3 M3	M3@
SIM Card Slot	3G@
Intel UMA	UMA@
VRAM Option	X76@
Intel SBA	SBA@
Intel AOAC	AOAC@
TPM	TPM@
GPU N13M	N13M@
GPU N13P	N13MP

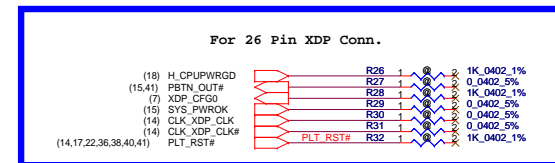
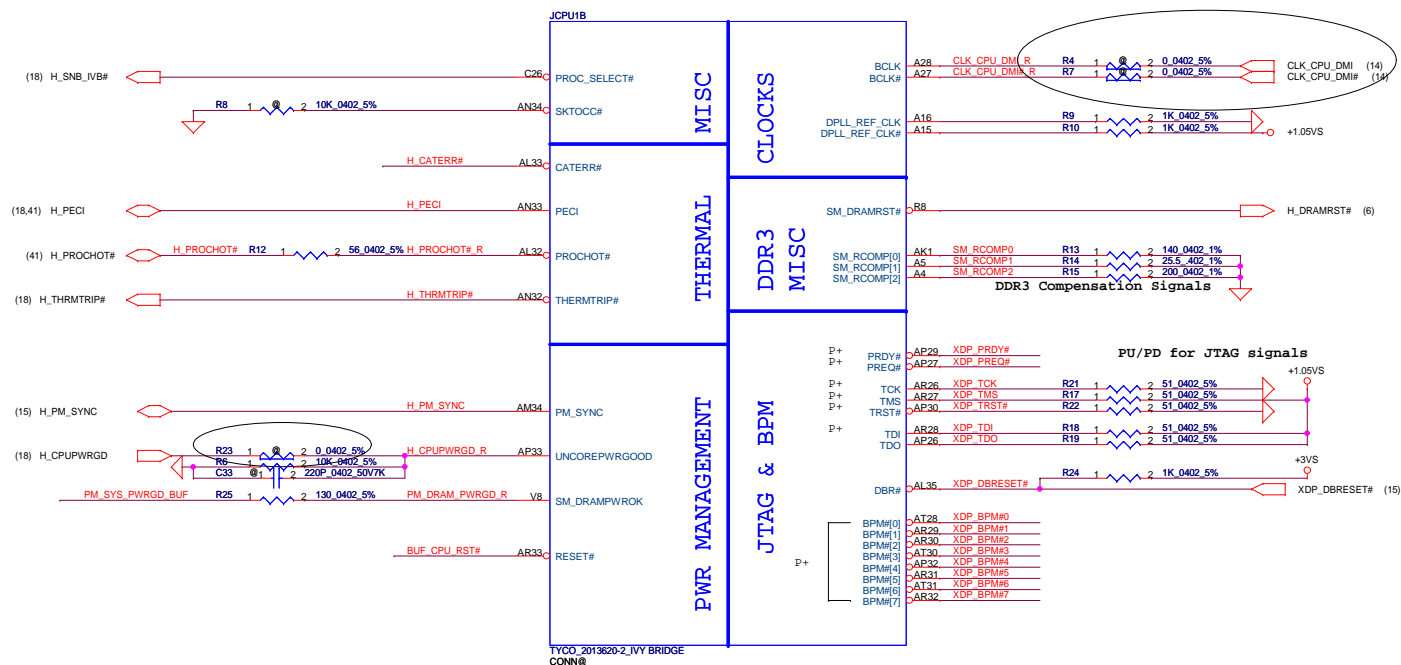
SMBUS Control Table

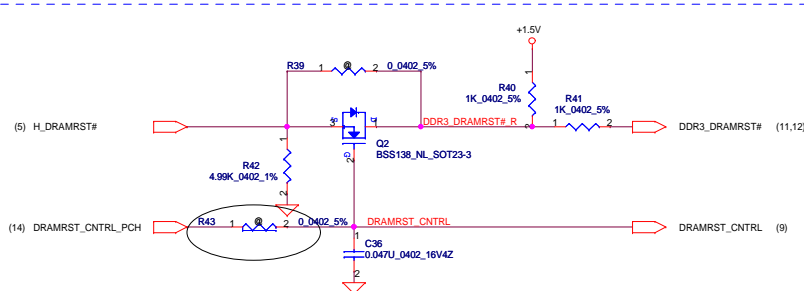
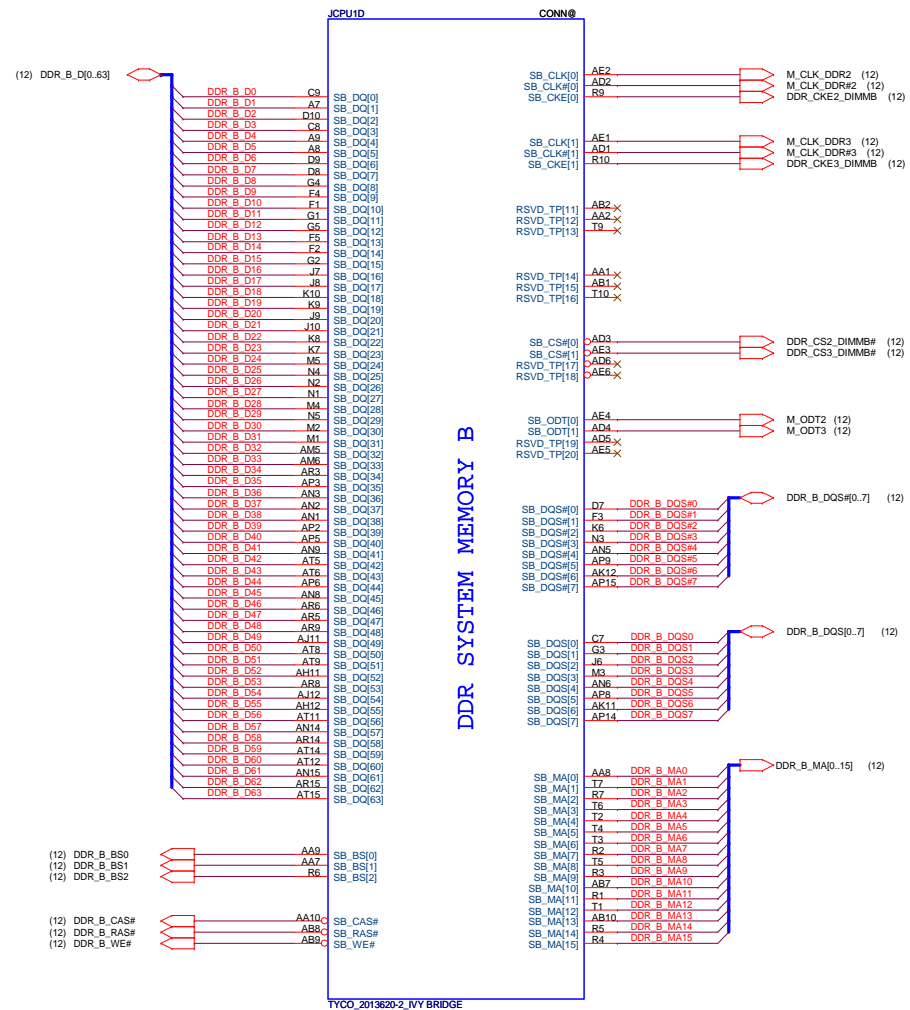
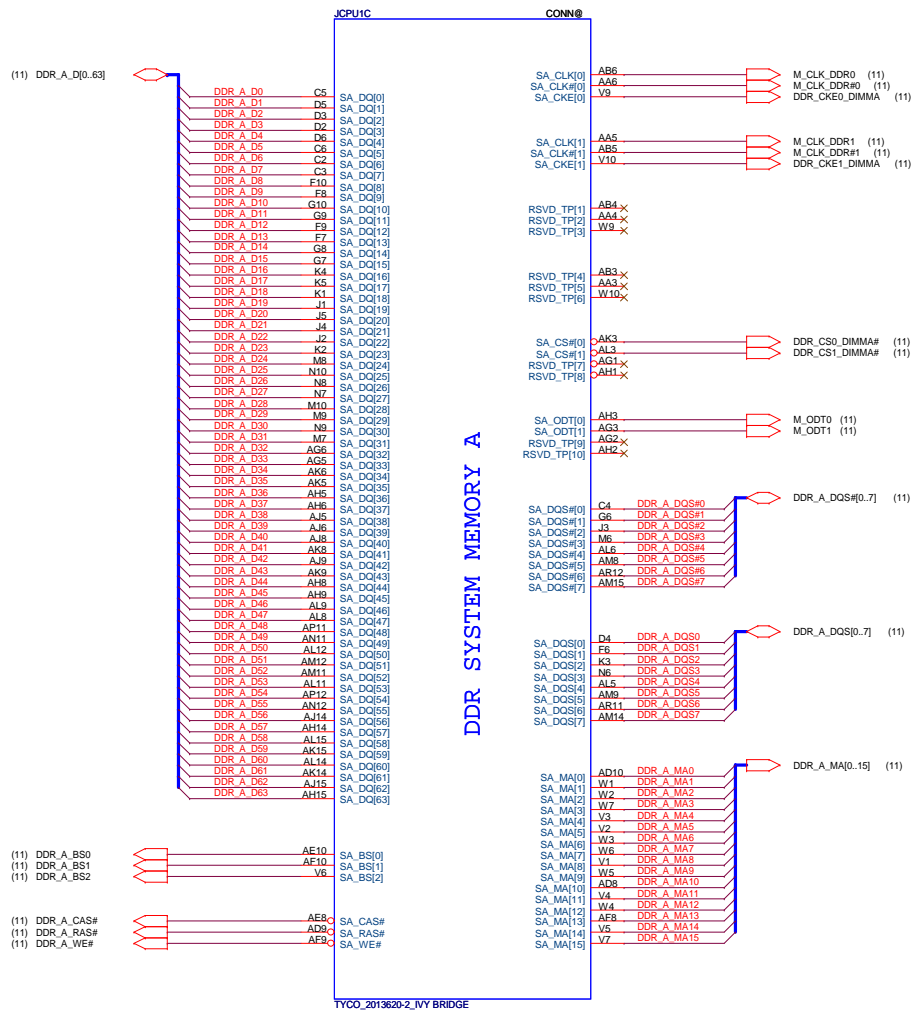
	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	✓	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	X	X	X	X	X	X	✓
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	X	X	X	✓	✓	X	X
SMBDATA	+3VALW				+3VS	+3VS		
SML0CLK	PCH	X	X	X	X	X	X	X
SML0DATA	+3VALW							
SML1CLK	PCH	✓	X	✓	X	X	✓	X
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

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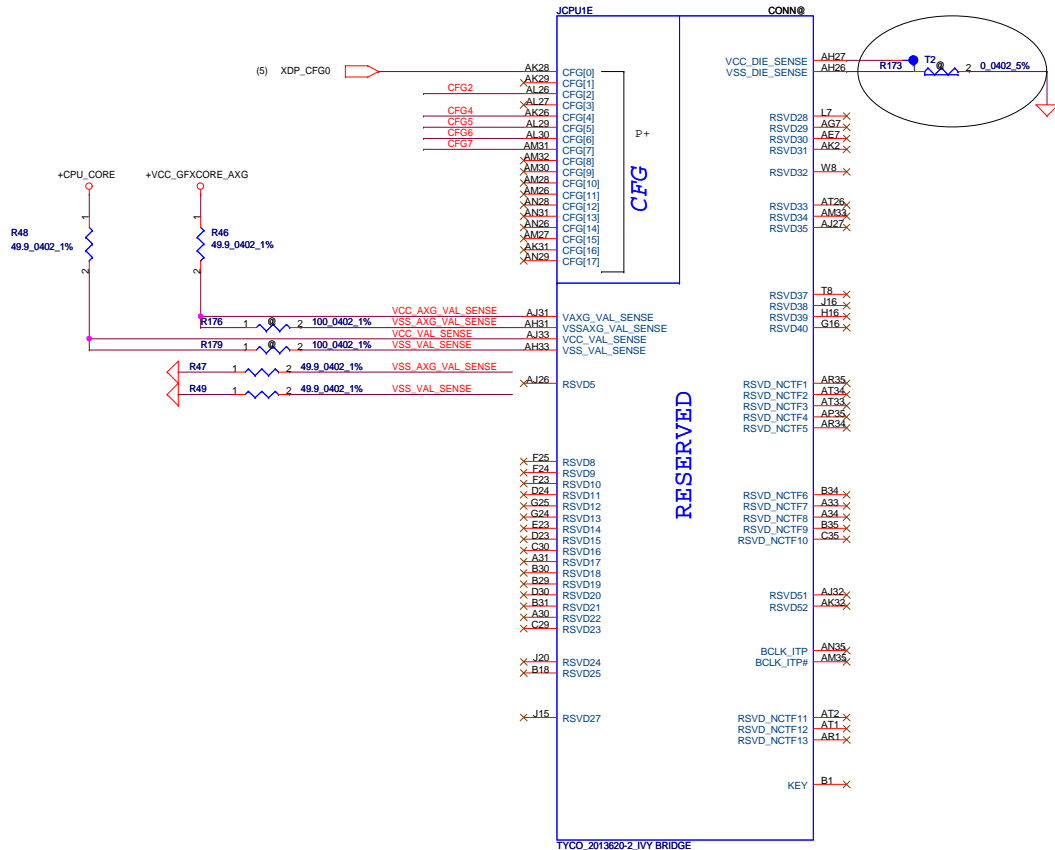


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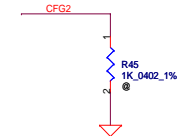




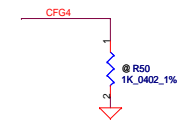
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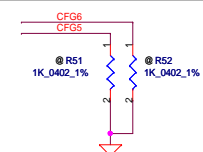
CFG Straps for Processor



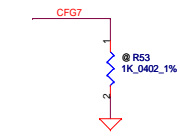
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	<p>* 1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>0: Lane Reversed</p>



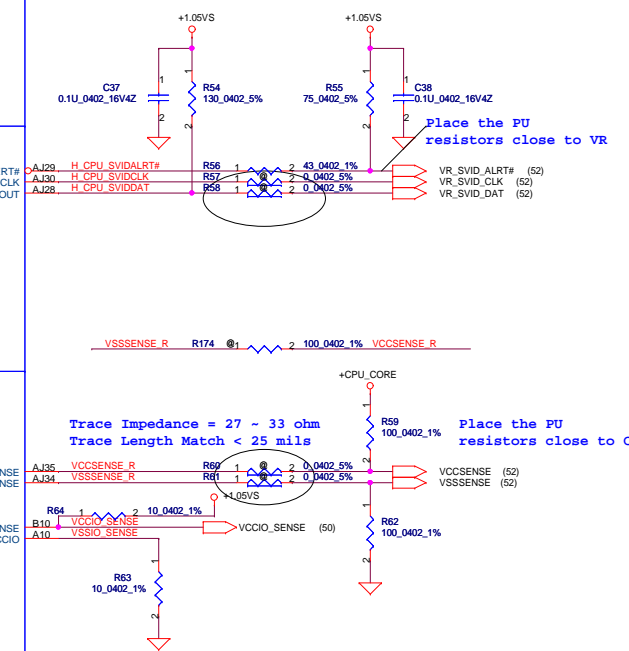
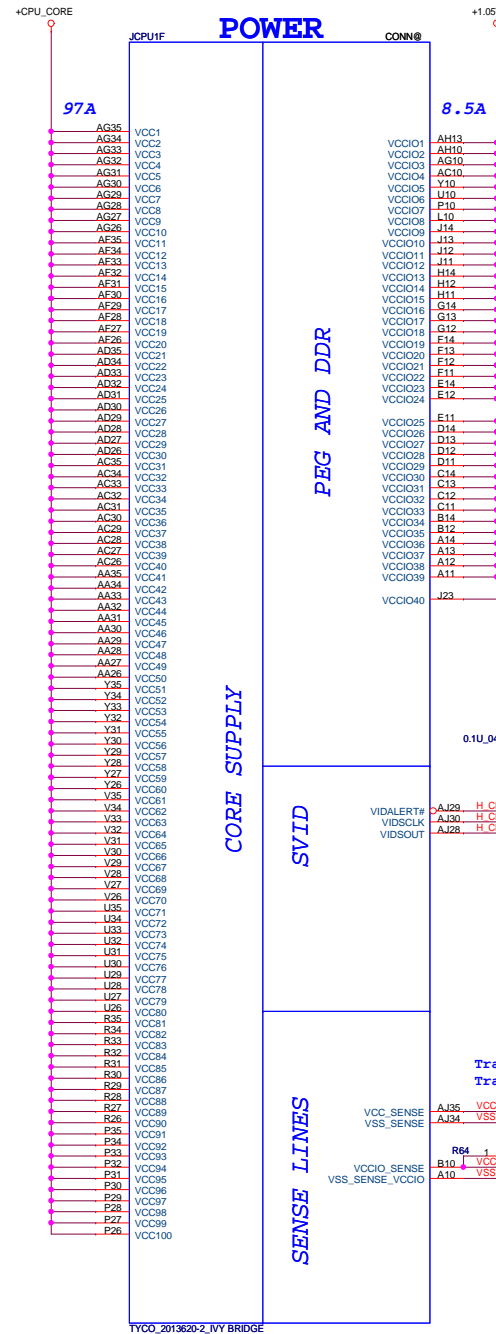
Display Port Presence Strap	
CFG4	<p>* 1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



PCIe Port Bifurcation Straps	
CFG[6:5]	<p>* 11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</p>

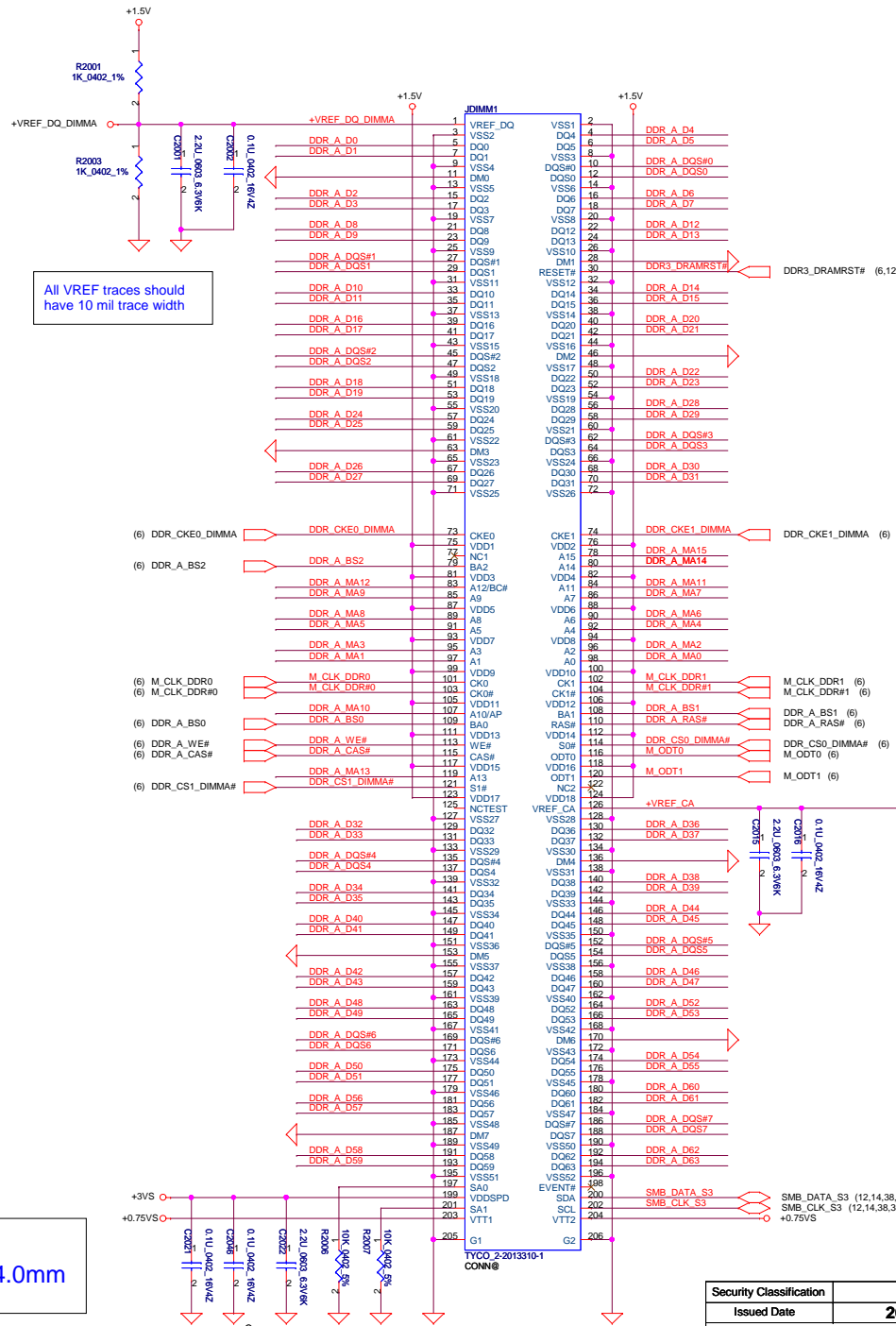


PEG DEFER TRAINING	
CFG7	<p>1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>



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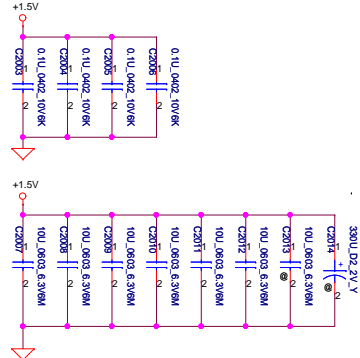


All VREF traces should have 10 mil trace width

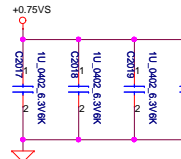
<Address: 00>
DIMM_A Reserve H:4.0mm

- DDR_A_DQS#0[0..7] (6)
- DDR_A_DQS#1[0..7] (6)
- DDR_A_D[0..63] (6)
- DDR_A_MA[0..15] (6)

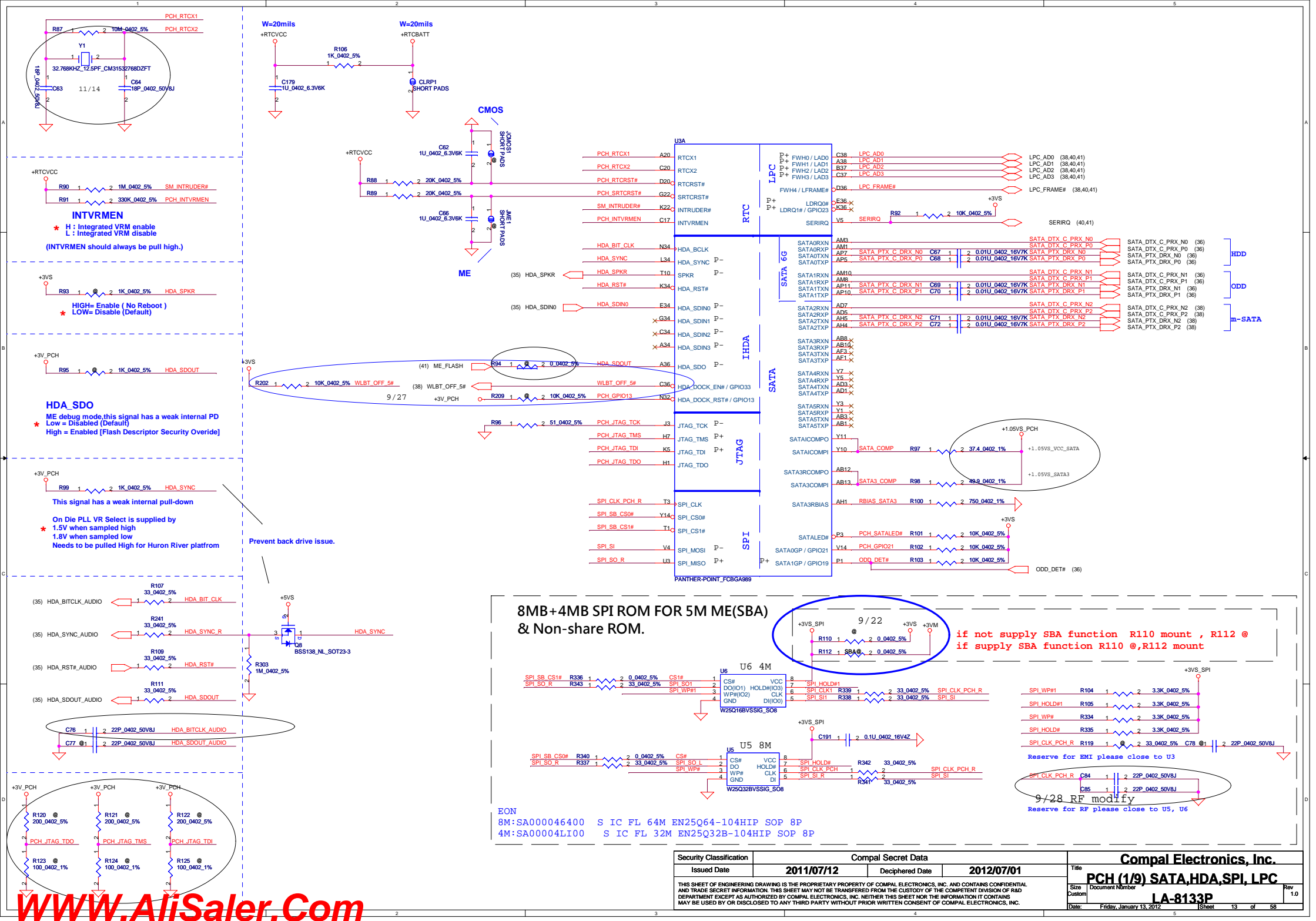
Layout Note:
Place near
JDIMM1

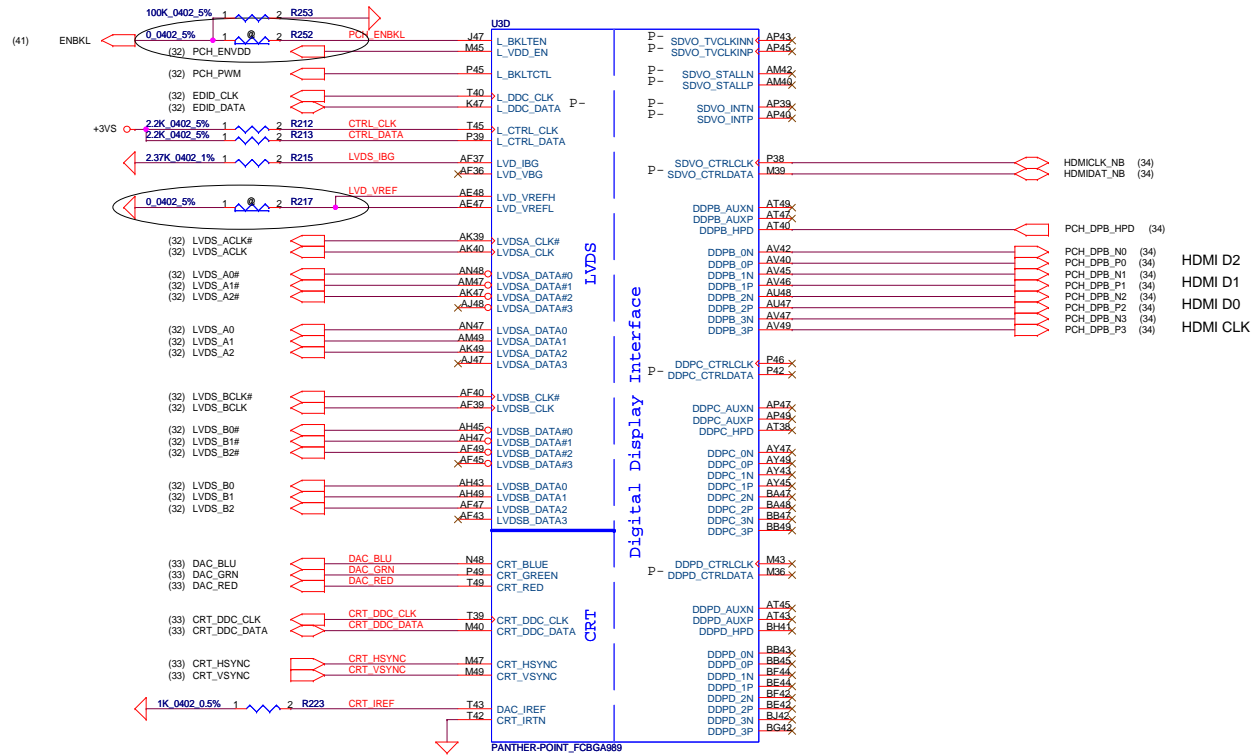


Layout Note:
Place near
JDIMM1.203,204

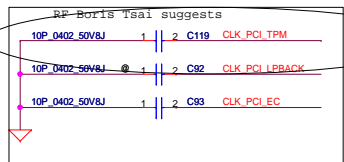
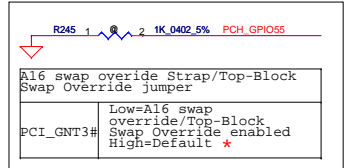
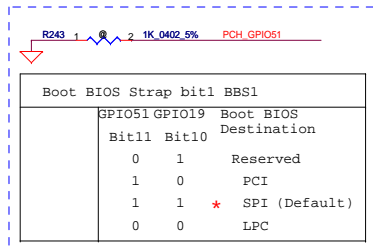
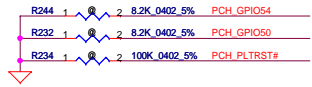
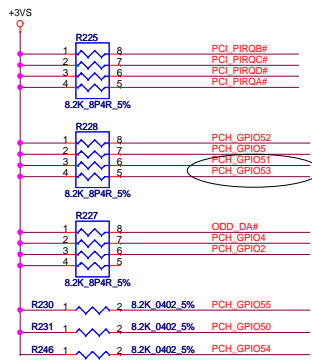


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- (37) USB3_RX1_N
- (37) USB3_RX2_N
- (37) USB3_RX3_N
- (37) USB3_RX1_P
- (37) USB3_RX2_P
- (37) USB3_RX3_P
- (37) USB3_TX1_N
- (37) USB3_TX2_N
- (37) USB3_TX3_N
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- (37) USB3_TX2_P
- (37) USB3_TX3_P

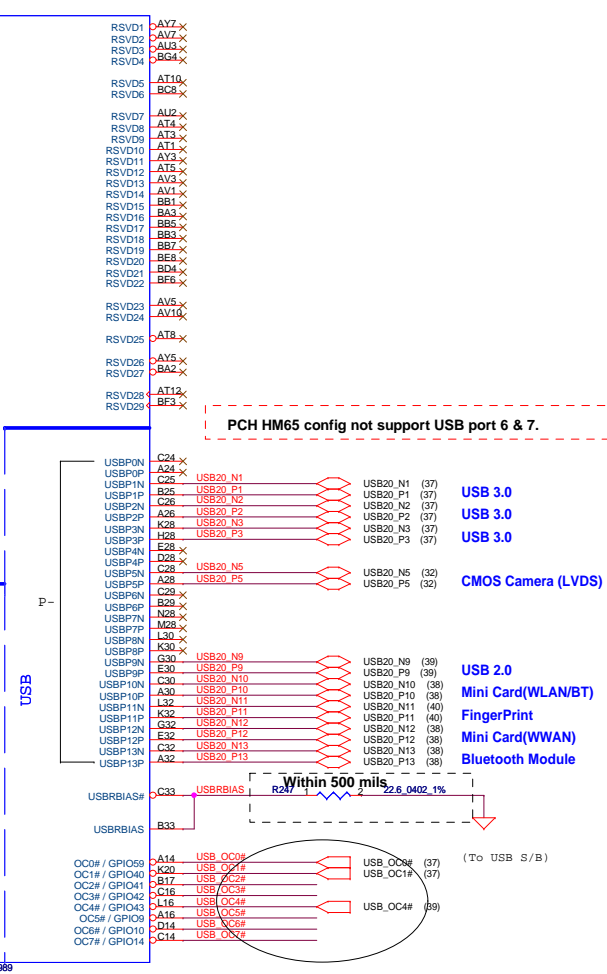
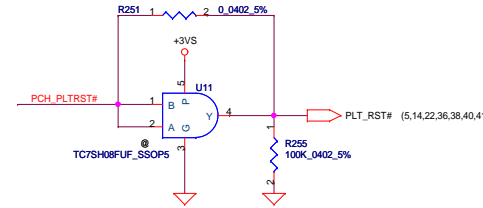
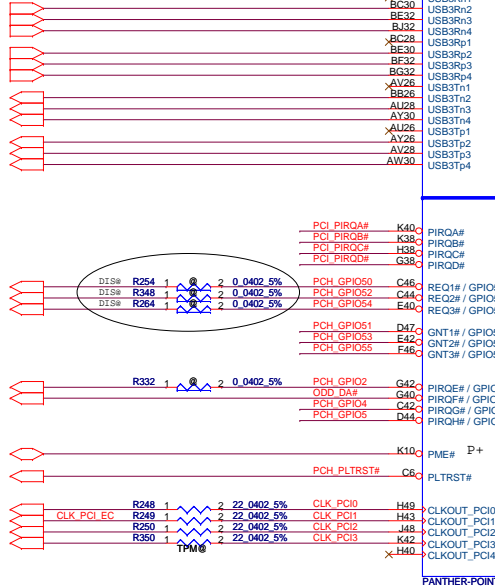
- (22) DGPU_HOLD_RST#
- (51) NVDD_PWR_EN
- (22,44) DGPU_PWR_EN

- (38) BT_DET#
- (36) ODD_DA#

- (41) PCI_PME#
- (5) PCH_PLTRST#

- (14) CLK_PCI_LPBACK
- (41) CLK_PCI_EC
- (38,40) CLK_PCI_DB
- (40) CLK_PCI_TPM

- 10P 0402 50V8J 1 2 C119 CLK_PCI_TPM
- 10P 0402 50V8J 1 2 C92 CLK_PCI_LPBACK
- 10P 0402 50V8J 1 2 C93 CLK_PCI_EC

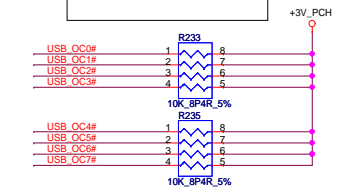


PCH HM65 config not support USB port 6 & 7.

USB 3.0
USB 3.0
USB 3.0
CMOS Camera (LVDS)

USB 2.0
Mini Card(WLAN/BT)
FingerPrint
Mini Card(WWAN)
Bluetooth Module

OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2

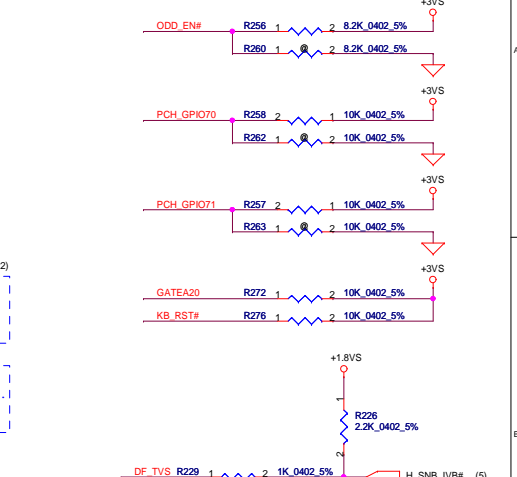
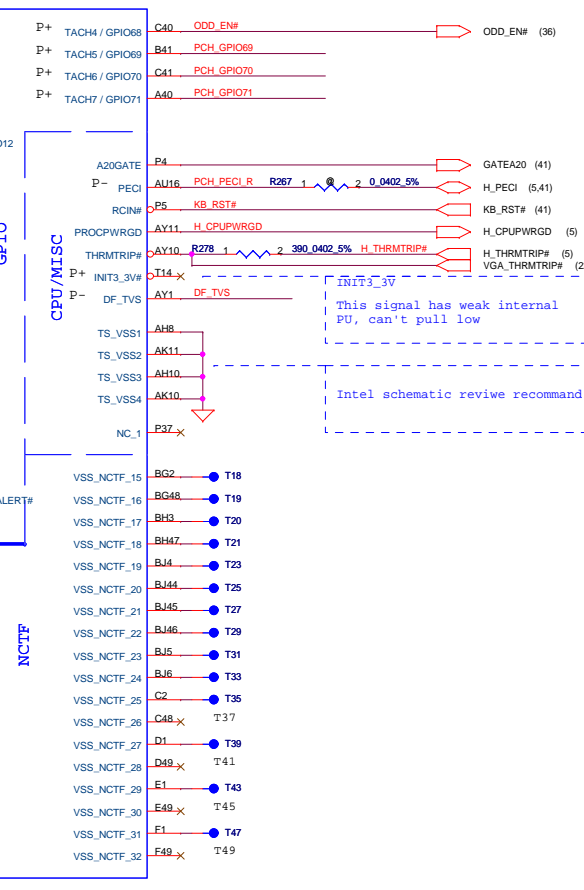
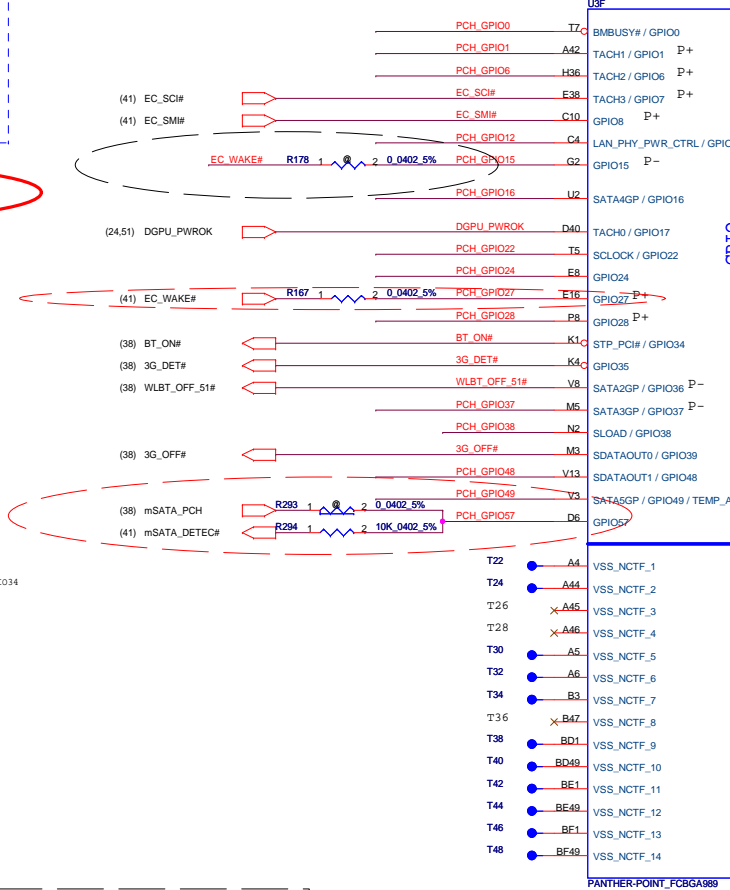
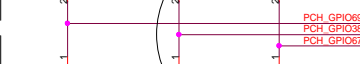
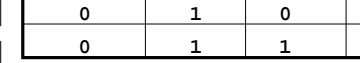
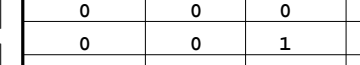
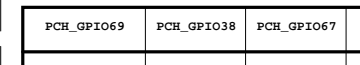
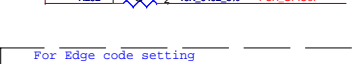
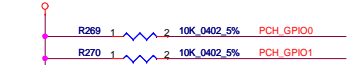
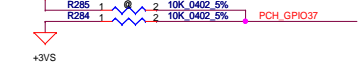
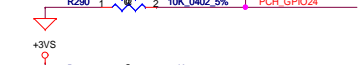
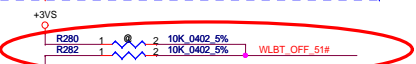
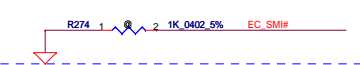


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GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



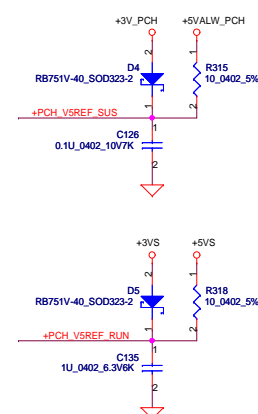
DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

CLOSE TO THE BRANCHING POINT

For Edge code setting

PCH_GPIO69	PCH_GPIO38	PCH_GPIO67	Function
0	0	0	Optimus
0	0	1	Reserved
0	1	0	DIS
0	1	1	UMA

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PCH (6/9) GPIO, CPU, MISC			Document Number
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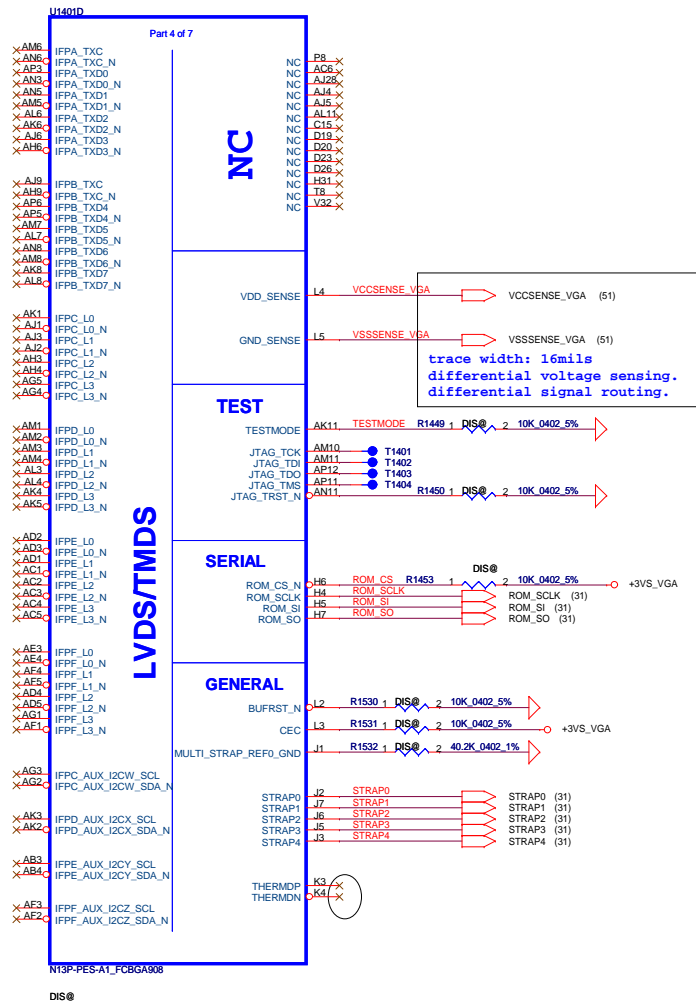
U3H		
H5	VSS[0]	
AA17	VSS[80]	AK38
AA2	VSS[81]	AK4
AA3	VSS[82]	AK42
AA33	VSS[83]	AK6
AA34	VSS[84]	AK9
AB11	VSS[85]	AL16
AB14	VSS[86]	AL17
AB30	VSS[87]	AL19
AB4	VSS[88]	AL2
AB43	VSS[89]	AL21
AB5	VSS[90]	AL23
AB7	VSS[91]	AL26
AC19	VSS[92]	AL27
AC2	VSS[93]	AL31
AC21	VSS[94]	AL33
AC24	VSS[95]	AL34
AC33	VSS[96]	AL48
AC34	VSS[97]	AM11
AC48	VSS[98]	AM14
AD10	VSS[99]	AM36
AD11	VSS[100]	AM39
AD12	VSS[101]	AM43
AD13	VSS[102]	AM45
AD19	VSS[103]	AM6
AD24	VSS[104]	AM7
AD26	VSS[105]	AN2
AD27	VSS[106]	AN29
AD3	VSS[107]	AN3
AD34	VSS[108]	AN31
AD36	VSS[109]	AP12
AD37	VSS[110]	AP19
AD38	VSS[111]	AP28
AD39	VSS[112]	AP30
AD4	VSS[113]	AP32
AD40	VSS[114]	AP36
AD42	VSS[115]	AP4
AD43	VSS[116]	AP42
AD45	VSS[117]	AP46
AD46	VSS[118]	AP8
AD8	VSS[119]	AR2
AE2	VSS[120]	AR48
AE3	VSS[121]	AT11
AE10	VSS[122]	AT13
AE12	VSS[123]	AT18
AD14	VSS[124]	AT22
AD16	VSS[125]	AT26
AE16	VSS[126]	AT28
AE19	VSS[127]	AT30
AE24	VSS[128]	AT32
AE26	VSS[129]	AT34
AE27	VSS[130]	AT39
AE29	VSS[131]	AT42
AE31	VSS[132]	AT46
AE38	VSS[133]	AT7
AE4	VSS[134]	AU24
AE42	VSS[135]	AU30
AE46	VSS[136]	AV16
AE5	VSS[137]	AV20
AE7	VSS[138]	AV24
AE8	VSS[139]	AV30
AG19	VSS[140]	AV38
AG2	VSS[141]	AV4
AG31	VSS[142]	AV43
AG48	VSS[143]	AV8
AH11	VSS[144]	AW14
AH3	VSS[145]	AW18
AH36	VSS[146]	AW2
AH39	VSS[147]	AW22
AH40	VSS[148]	AW26
AH42	VSS[149]	AW28
AH46	VSS[150]	AW32
AH7	VSS[151]	AW34
AJ19	VSS[152]	AW36
AJ21	VSS[153]	AW40
AJ24	VSS[154]	AW46
AJ33	VSS[155]	AV11
AJ34	VSS[156]	AY12
AK12	VSS[157]	AY22
AK	VSS[158]	AY28

PANTHER-POINT_FCBGA989

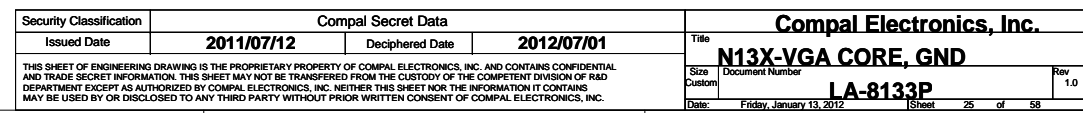
U3I		
AY4	VSS[159]	
AY42	VSS[160]	AY4
AY46	VSS[161]	AY46
AY8	VSS[162]	AY8
B11	VSS[163]	B11
B15	VSS[164]	B15
B19	VSS[165]	B19
B23	VSS[166]	B23
B27	VSS[167]	B27
B31	VSS[168]	B31
B35	VSS[169]	B35
B39	VSS[170]	B39
B7	VSS[171]	B7
F45	VSS[172]	F45
BB12	VSS[173]	BB12
BB16	VSS[174]	BB16
BB20	VSS[175]	BB20
BB22	VSS[176]	BB22
BB24	VSS[177]	BB24
BB28	VSS[178]	BB28
BB30	VSS[179]	BB30
BB38	VSS[180]	BB38
BB4	VSS[181]	BB4
BB46	VSS[182]	BB46
BC14	VSS[183]	BC14
BC18	VSS[184]	BC18
BC2	VSS[185]	BC2
BC22	VSS[186]	BC22
BC26	VSS[187]	BC26
BC32	VSS[188]	BC32
BC34	VSS[189]	BC34
BC36	VSS[190]	BC36
BC40	VSS[191]	BC40
BC42	VSS[192]	BC42
BC48	VSS[193]	BC48
BD46	VSS[194]	BD46
BD5	VSS[195]	BD5
BE22	VSS[196]	BE22
BE40	VSS[197]	BE40
BF10	VSS[198]	BF10
BF12	VSS[199]	BF12
BF16	VSS[200]	BF16
BF20	VSS[201]	BF20
BF22	VSS[202]	BF22
BF24	VSS[203]	BF24
BF26	VSS[204]	BF26
BF28	VSS[205]	BF28
BF30	VSS[206]	BF30
BF32	VSS[207]	BF32
BF38	VSS[208]	BF38
BF40	VSS[209]	BF40
BF4	VSS[210]	BF4
BG17	VSS[211]	BG17
BG21	VSS[212]	BG21
BG33	VSS[213]	BG33
BG44	VSS[214]	BG44
BG8	VSS[215]	BG8
BH11	VSS[216]	BH11
BH15	VSS[217]	BH15
BH17	VSS[218]	BH17
BH19	VSS[219]	BH19
BH10	VSS[220]	BH10
BH27	VSS[221]	BH27
BH31	VSS[222]	BH31
BH33	VSS[223]	BH33
BH35	VSS[224]	BH35
BH39	VSS[225]	BH39
BH43	VSS[226]	BH43
BH7	VSS[227]	BH7
D3	VSS[228]	D3
D12	VSS[229]	D12
D16	VSS[230]	D16
D18	VSS[231]	D18
D22	VSS[232]	D22
D24	VSS[233]	D24
D26	VSS[234]	D26
D28	VSS[235]	D28
D30	VSS[236]	D30
D32	VSS[237]	D32
D34	VSS[238]	D34
D38	VSS[239]	D38
D42	VSS[240]	D42
D46	VSS[241]	D46
E8	VSS[242]	E8
G18	VSS[243]	G18
G20	VSS[244]	G20
G28	VSS[245]	G28
G28	VSS[246]	G28
G28	VSS[247]	G28
G28	VSS[248]	G28
G28	VSS[249]	G28
H12	VSS[250]	H12
H18	VSS[251]	H18
H22	VSS[252]	H22
H24	VSS[253]	H24
H26	VSS[254]	H26
H32	VSS[255]	H32
H34	VSS[256]	H34
H34	VSS[257]	H34
H34	VSS[258]	H34

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H46	VSS[259]	
K18	VSS[260]	K18
K26	VSS[261]	K26
K30	VSS[262]	K30
K46	VSS[263]	K46
K7	VSS[264]	K7
L18	VSS[265]	L18
L20	VSS[266]	L20
L26	VSS[267]	L26
L28	VSS[268]	L28
L38	VSS[269]	L38
L46	VSS[270]	L46
M12	VSS[271]	M12
M16	VSS[272]	M16
M22	VSS[273]	M22
M24	VSS[274]	M24
M30	VSS[275]	M30
M32	VSS[276]	M32
M34	VSS[277]	M34
M38	VSS[278]	M38
M42	VSS[279]	M42
M46	VSS[280]	M46
M8	VSS[281]	M8
N18	VSS[282]	N18
N18	VSS[283]	N18
N18	VSS[284]	N18
N18	VSS[285]	N18
N18	VSS[286]	N18
N18	VSS[287]	N18
N18	VSS[288]	N18
N18	VSS[289]	N18
N18	VSS[290]	N18
N18	VSS[291]	N18
N18	VSS[292]	N18
N18	VSS[293]	N18
N18	VSS[294]	N18
N18	VSS[295]	N18
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N18	VSS[299]	N18
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N18	VSS[302]	N18
N18	VSS[303]	N18
N18	VSS[304]	N18
N18	VSS[305]	N18
N18	VSS[306]	N18
N18	VSS[307]	N18
N18	VSS[308]	N18
N18	VSS[309]	N18
N18	VSS[310]	N18
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N18	VSS[316]	N18
N18	VSS[317]	N18
N18	VSS[318]	N18
N18	VSS[319]	N18
N18	VSS[320]	N18
N18	VSS[321]	N18
N18	VSS[322]	N18
N18	VSS[323]	N18
N18	VSS[324]	N18
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N18	VSS[329]	N18
N18	VSS[330]	N18
N18	VSS[331]	N18
N18	VSS[332]	N18
N18	VSS[333]	N18
N18	VSS[334]	N18
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N18	VSS[336]	N18
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N18	VSS[341]	N18
N18	VSS[342]	N18
N18	VSS[343]	N18
N18	VSS[344]	N18
N18	VSS[345]	N18
N18	VSS[346]	N18
N18	VSS[347]	N18
N18	VSS[348]	N18
N18	VSS[349]	N18
N18	VSS[350]	N18
N18	VSS[351]	N18
N18	VSS[352]	N18

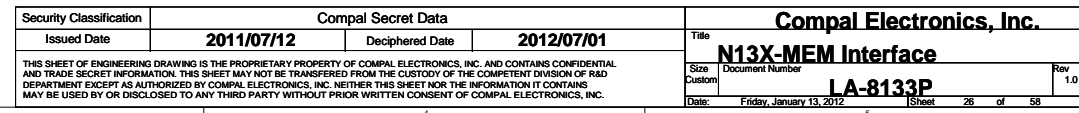
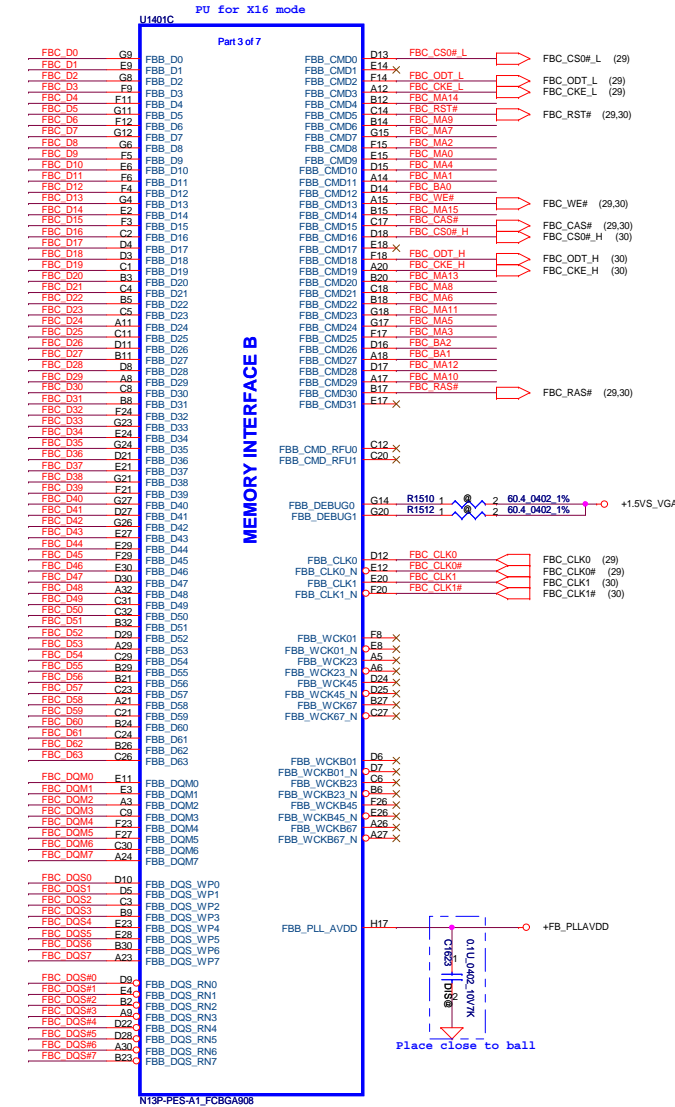


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				Rev	1.0

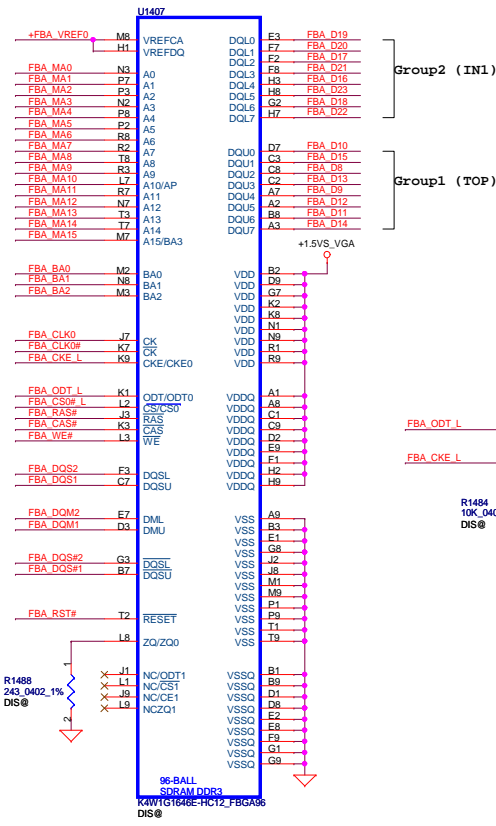
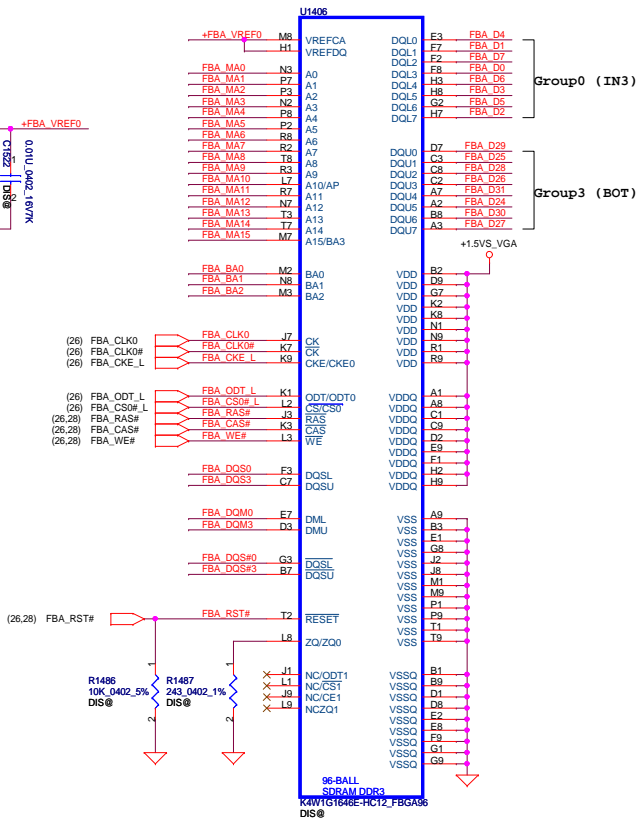
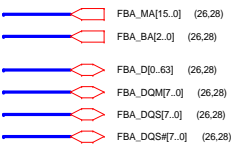




	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

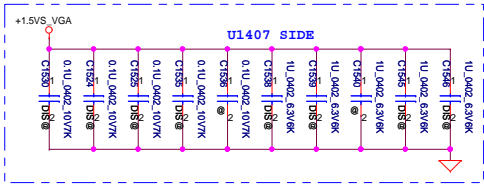
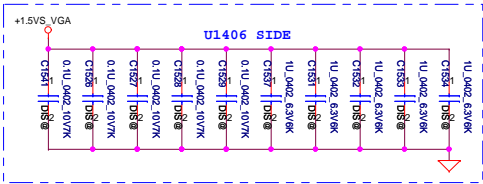


Memory Partition A - Lower 32 bits

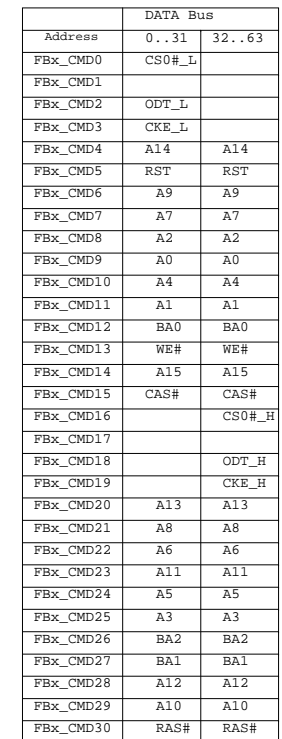
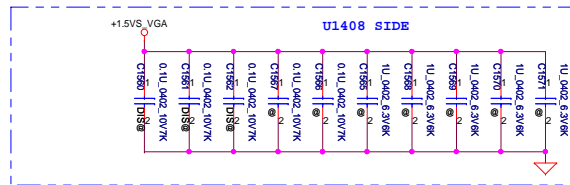
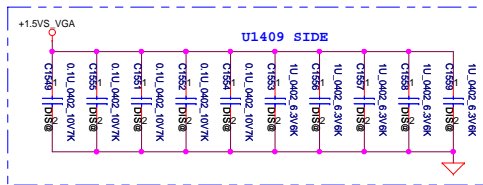


Mode D - Mirror Mode Mapping

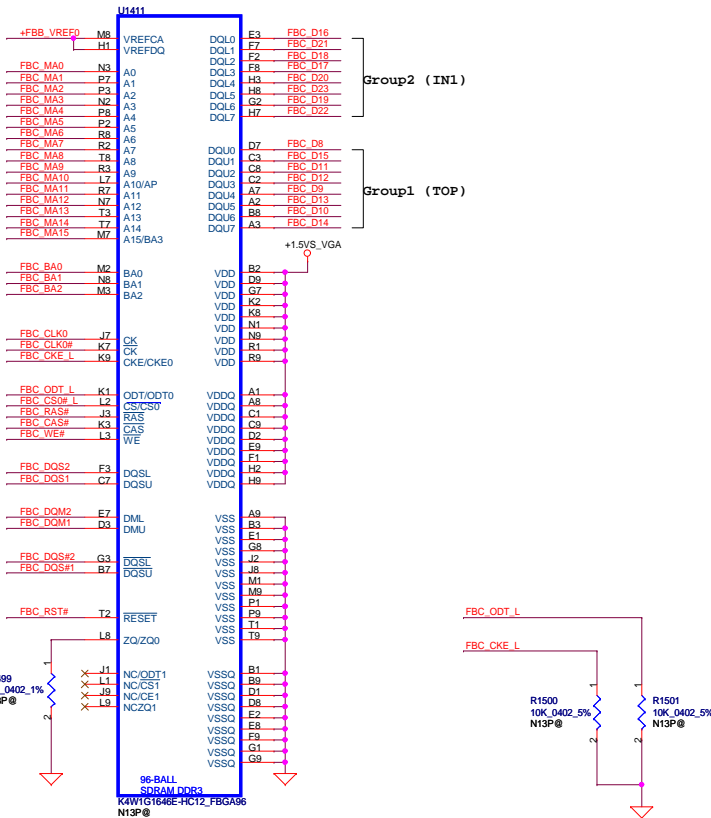
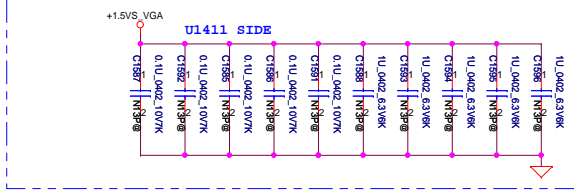
DATA Bus	
Address	0..31 32..63
FBx_CMD0	CS0#_L
FBx_CMD1	
FBx_CMD2	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14 A14
FBx_CMD5	RST RST
FBx_CMD6	A9 A9
FBx_CMD7	A7 A7
FBx_CMD8	A2 A2
FBx_CMD9	A0 A0
FBx_CMD10	A4 A4
FBx_CMD11	A1 A1
FBx_CMD12	BA0 BA0
FBx_CMD13	WE# WE#
FBx_CMD14	A15 A15
FBx_CMD15	CAS# CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	
FBx_CMD18	ODT_H
FBx_CMD19	CKE_H
FBx_CMD20	A13 A13
FBx_CMD21	A8 A8
FBx_CMD22	A6 A6
FBx_CMD23	A11 A11
FBx_CMD24	A5 A5
FBx_CMD25	A3 A3
FBx_CMD26	BA2 BA2
FBx_CMD27	BA1 BA1
FBx_CMD28	A12 A12
FBx_CMD29	A10 A10
FBx_CMD30	RAS# RAS#



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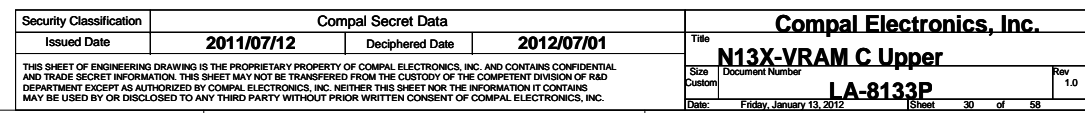
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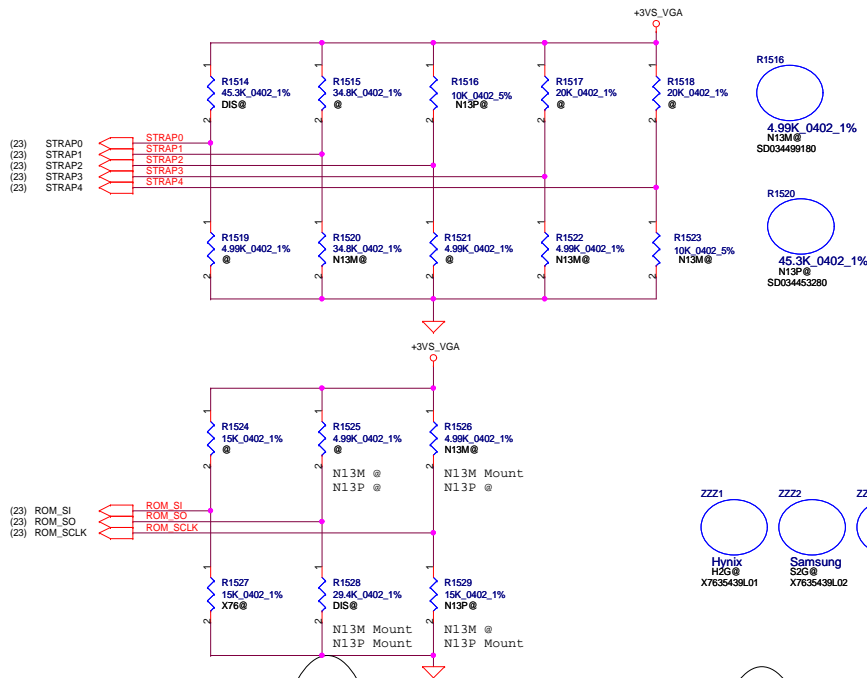


	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

USER Straps	
User[3:0]	
1000-1100	Customer defined

PCIE_MAX_SPEED	
0	Limit to PCIe Gen1
1	PCIe Gen 2/3 Capable

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GL	Samsung 900MHz	K4W1G1646G-BC11	PD 10K	PD 15K	PD 20K	PU 45K	PD 45K	PU 10K	NC	NC
		64Mx16						PU 45K(ES)		
	Hynix 900MHz	H5TQ1G63DFR-11C	PD 10K	PD 15K	PD 15K	PU 45K	PD 45K	PU 10K	NC	NC
		64Mx16						PU 45K(ES)		
	Samsung 900MHz	K4W2G1646C-HC11	PD 10K	PD 15K	PD 45K	PU 45K	PD 45K	PU 10K	NC	NC
		128Mx16						PU 45K(ES)		
	Hynix 900MHz	H5TQ2G63BFR-11C	PD 10K	PD 15K	PD 35K	PU 45K	PD 45K	PU 10K	NC	NC
		128Mx16						PU 45K(ES)		

GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13M-GE1	Samsung 900MHz	K4W1G1646G-BC11	PD 30K	PU 5K	PD 20K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
		64Mx16								
	Hynix 900MHz	H5TQ1G63DFR-11C	PD 30K	PU 5K	PD 15K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
		64Mx16								
	Samsung 900MHz	K4W2G1646C-HC11	PD 30K	PU 5K	PD 45K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
		128Mx16								
	Hynix 900MHz	H5TQ2G63BFR-11C	PD 30K	PU 5K	PD 35K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
		128Mx16								

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from 15K to 5K

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				LA-8133P	

(16) DAC_RED
(16) DAC_GRN
(16) DAC_BLU

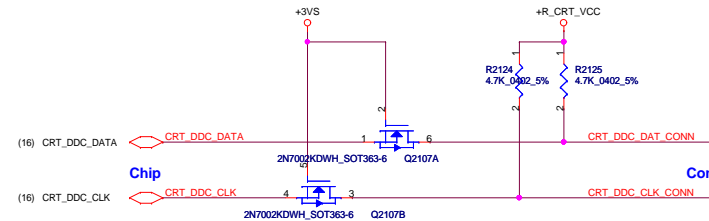
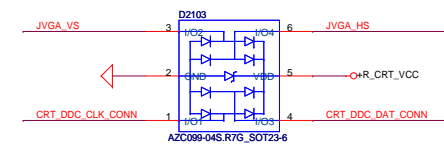
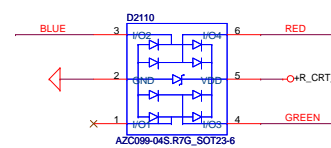
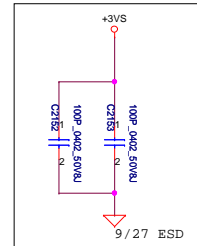
DAC_RED
DAC_GRN
DAC_BLU

(16) CRT_HSYNC

CRT_HSYNC

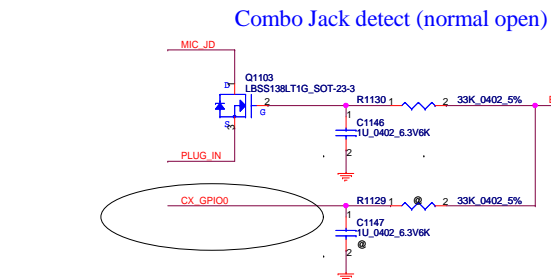
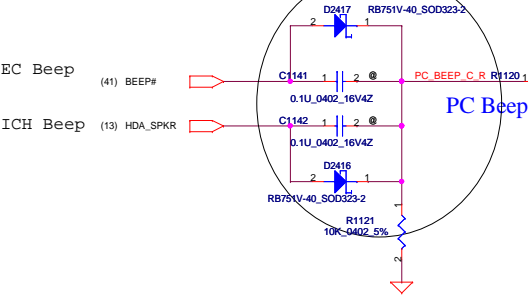
(16) CRT_VSYNC

CRT_VSYNC



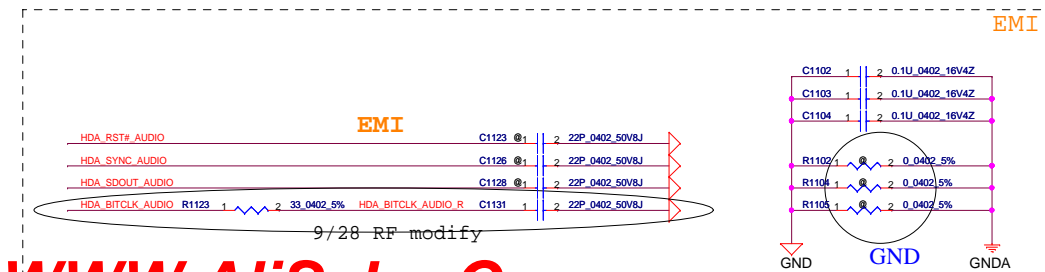
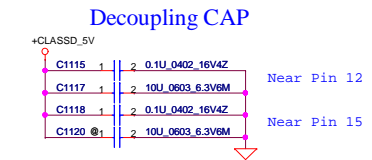
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	CRT Connector
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				Date	Friday, January 13, 2012
				Sheet	33 of 58
				Rev	1.0

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



Internal DMIC

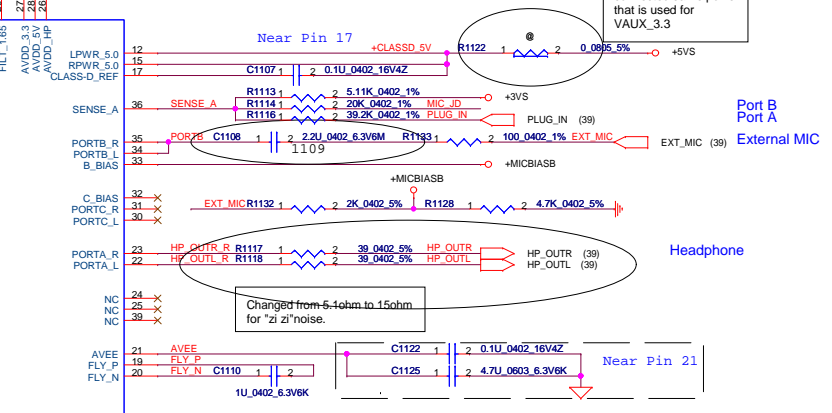
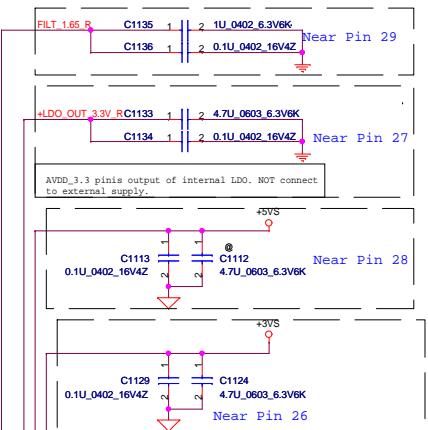
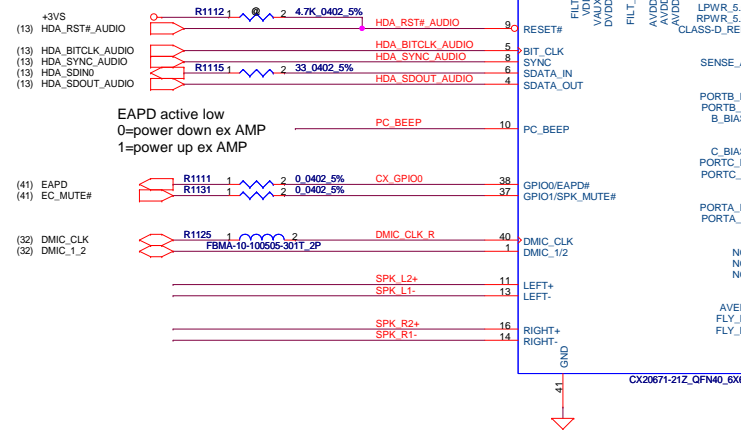
Internal SPEAKER



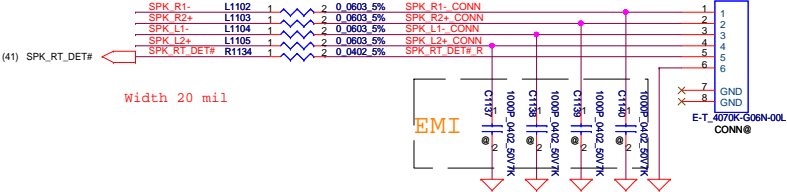
Layout Note: Path from +5VS to Pin12,
Pin15 must be very low
resistance (<0.01 ohms)

To support Wake-on-Jack or Wake-on-Ring, the CODEC
VAUX_3.3 & VDD_IO pins must be powered by a rail that
is not removed unless AC power is removed.
*DSH page42 has more detail.

10K only needed if supply to VAUX_3.3
is removed during system re-start.



EMC request
Bead 120ohm on these signals
Compal PN: SM010016720
Vendor PN: FBMA-L11-160808-121LMT
Rdc < 0.05 ohms
Rated Current > 2A



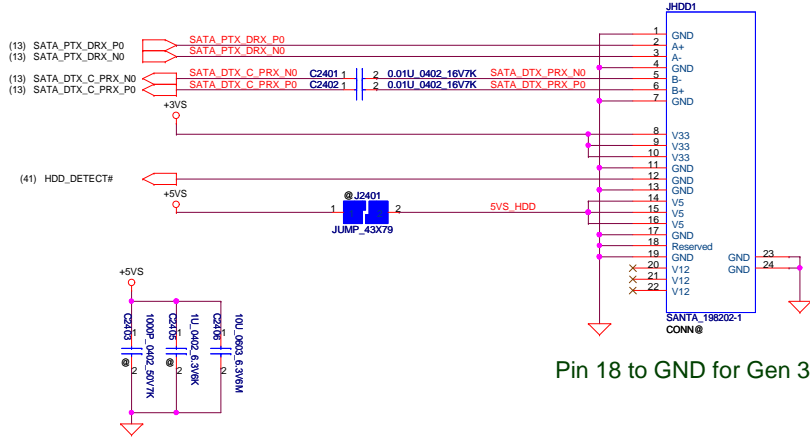
Internal Speaker

SP02000N010
SP02000SM10

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	HD Audio Codec CX20671
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				Custom	LA-8133P
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SATA HDD CONN.

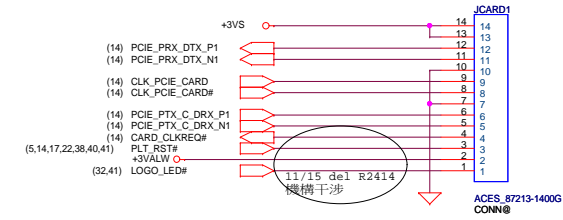
PN:DC010004C00



Pin 18 to GND for Gen 3

Card Reader CONN.

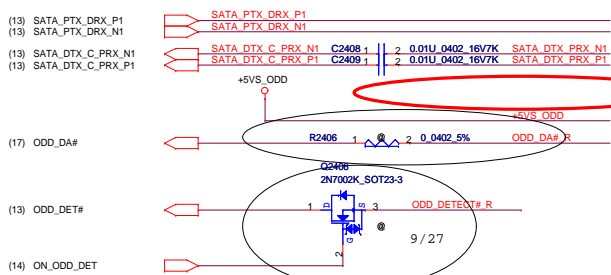
PN:SP01001BF00



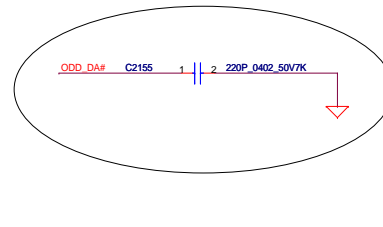
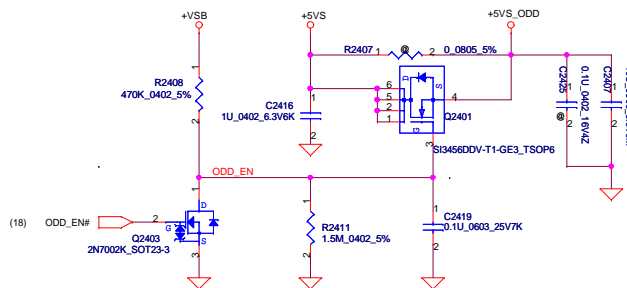
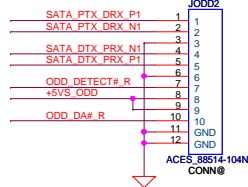
10/06
change PN to SP02000H810
footprint: ACES_87213-1400G_14P

SATA ODD CONN.

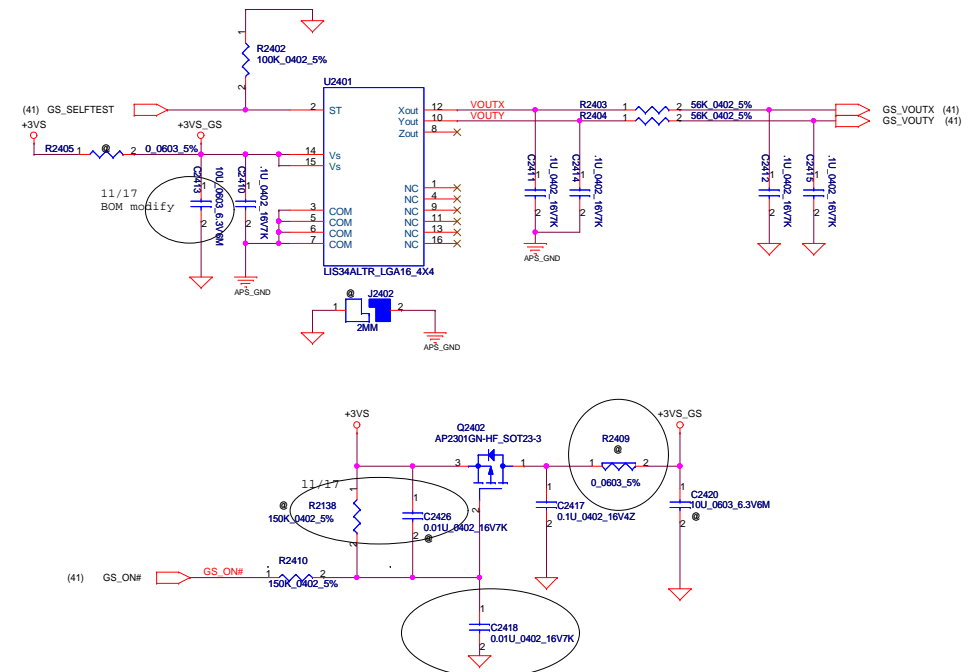
PN:SP01000TU10



for Edge 15'



APS G-Sensor



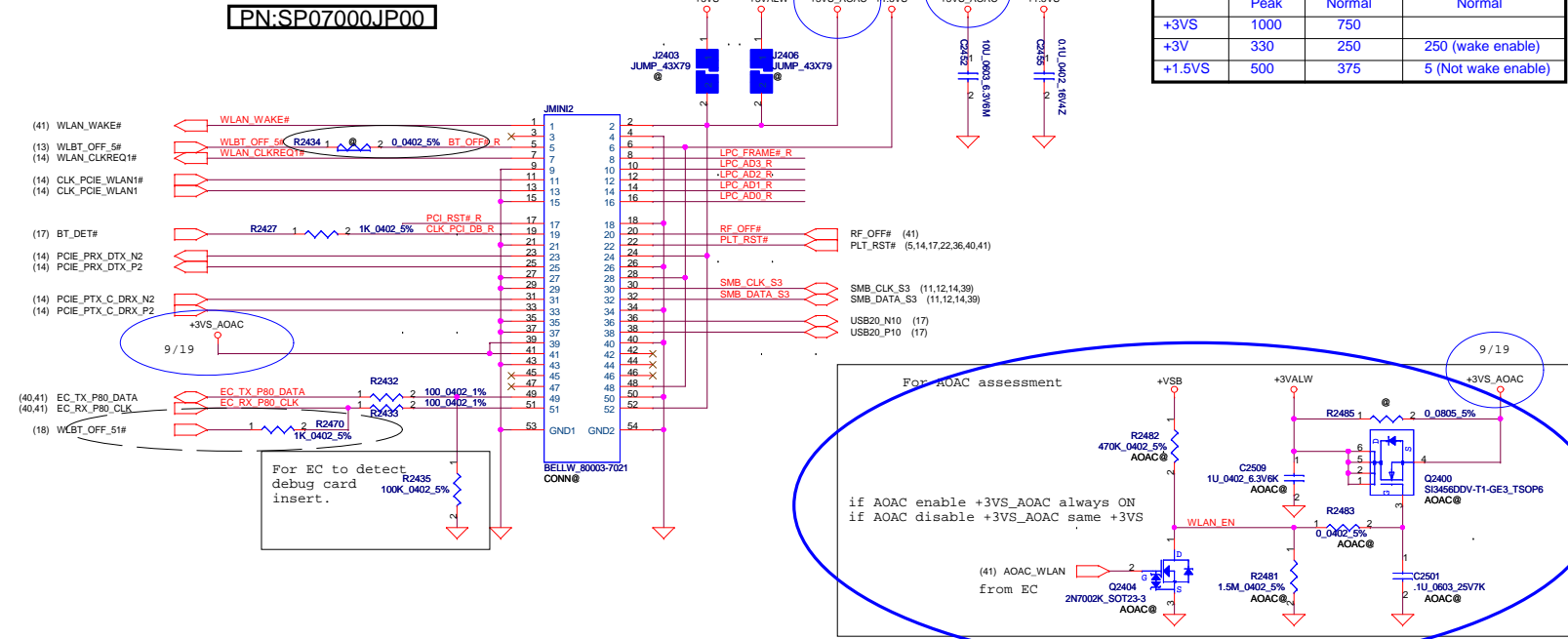
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	HDD/ODD/Card reader/G-Sensor	
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				Date:	Friday, January 13, 2012	Sheet

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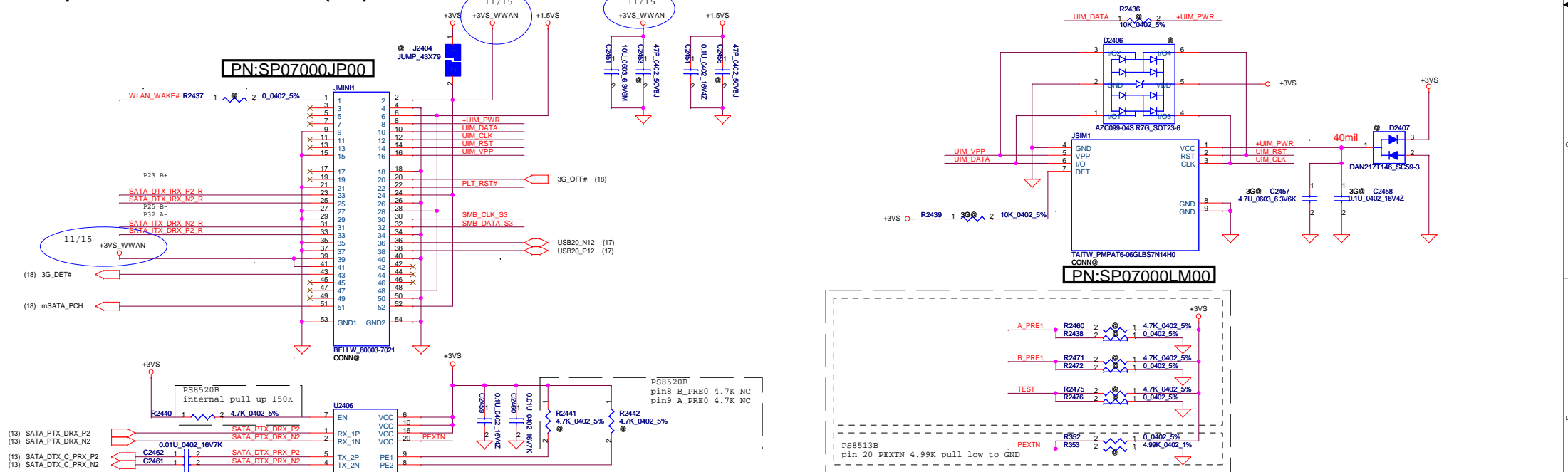
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	USB 3.0 Connector	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
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Mini-Express Card for WLAN/WiMAX(Half)

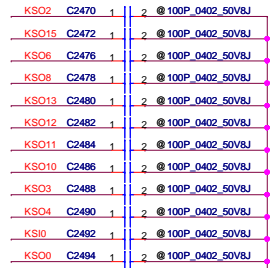
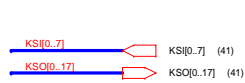
Mini-Express Card(WLAN/WiMAX)



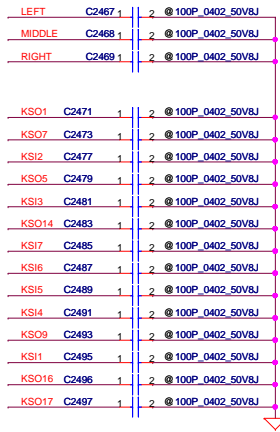
Mini-Express Card for WWAN/mSATA(Full)



INT_KBD Conn.



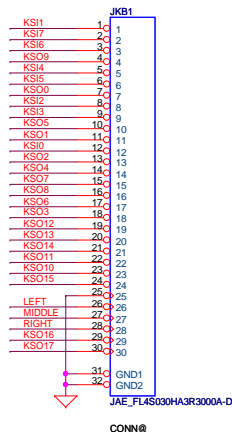
CONN PIN define need double check



Reserve for ESD.

M1(Left BUTTON)
M2(Center BUTTON)
M3(Right BUTTON)

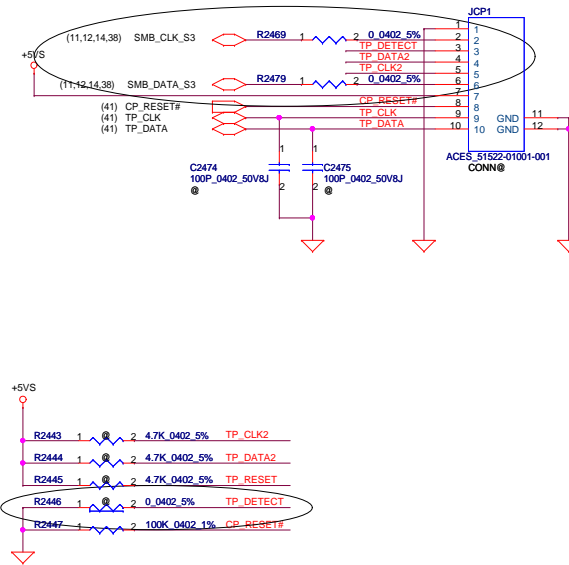
PN:SP01000YH00



CONN@

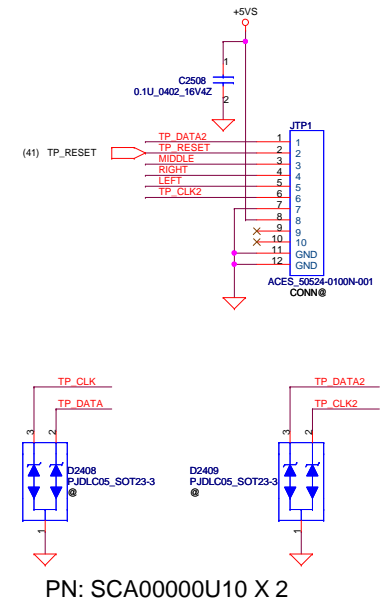
Click pad

PN:SP01001AL00



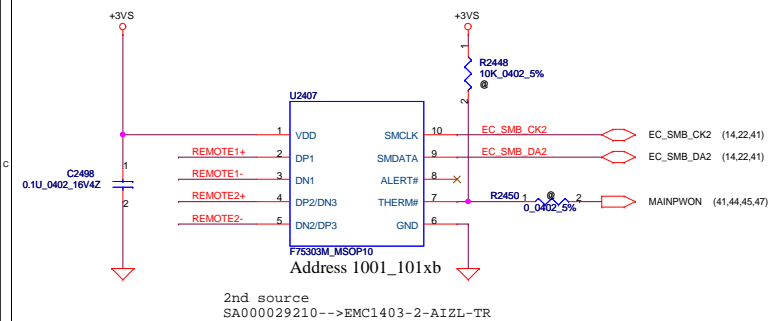
Track point

PN:SP01001CH00



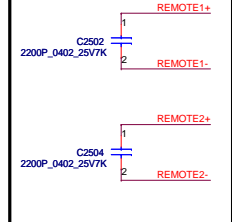
PN: SCA00000U10 X 2

Fintek thermal sensor placed near by TOP DDR3

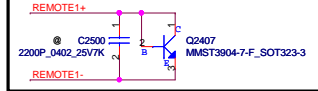


2nd source
SA000029210-->EMC1403-2-AIZL-TR

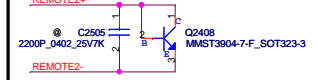
Close U2407



BOTTOM DDR3

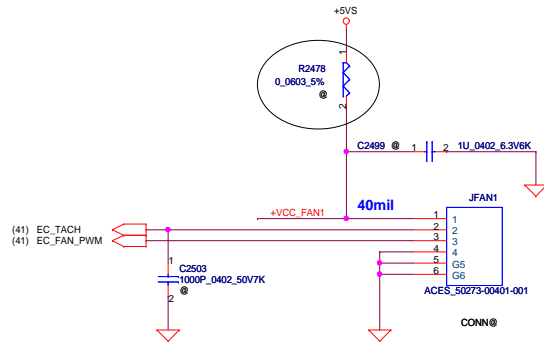


TOP CPU_CORE



REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

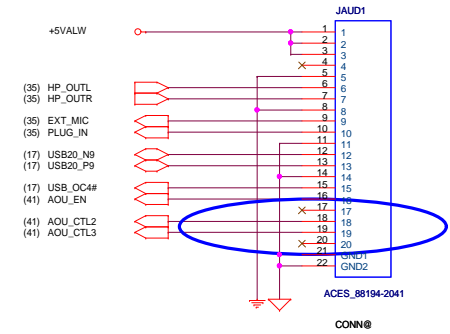
FAN CONN.



PN:SP02000U900

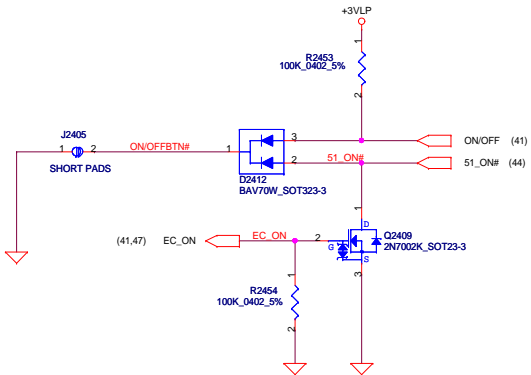
Audio Board

PN:SP011108040

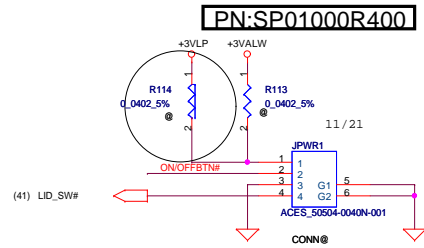


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Date: Friday, January 13, 2012				Sheet 39	of 58

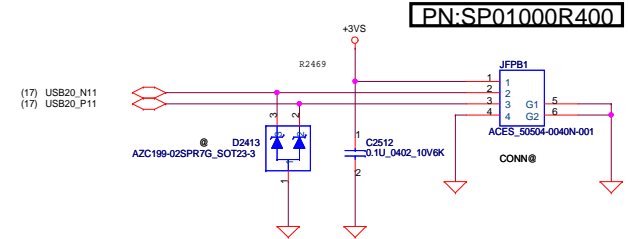
Power Button



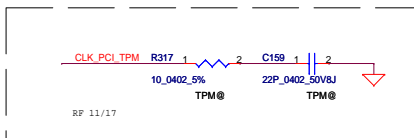
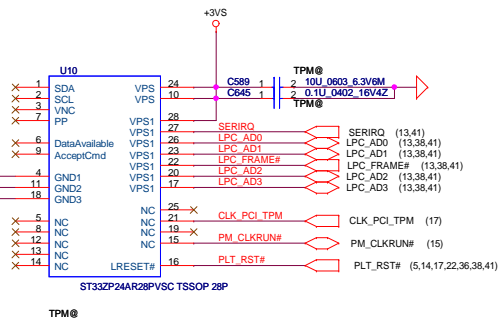
Power Button CONN.



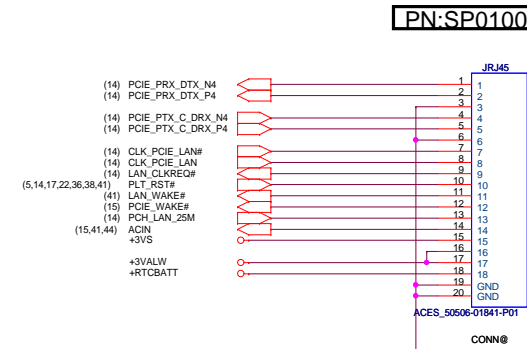
Finger Print Board



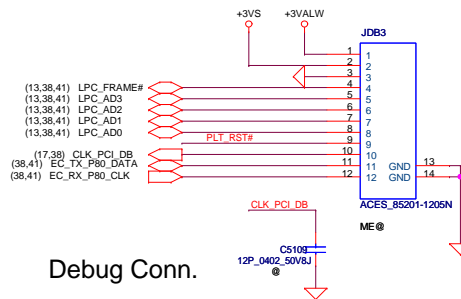
TPM



RJ45 Board



Debug Conn.

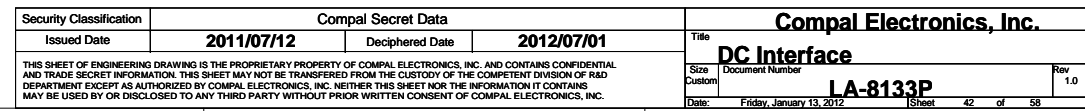
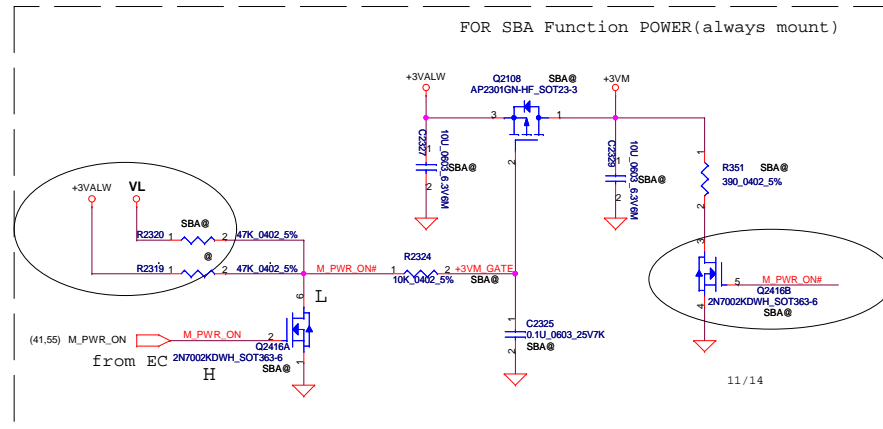
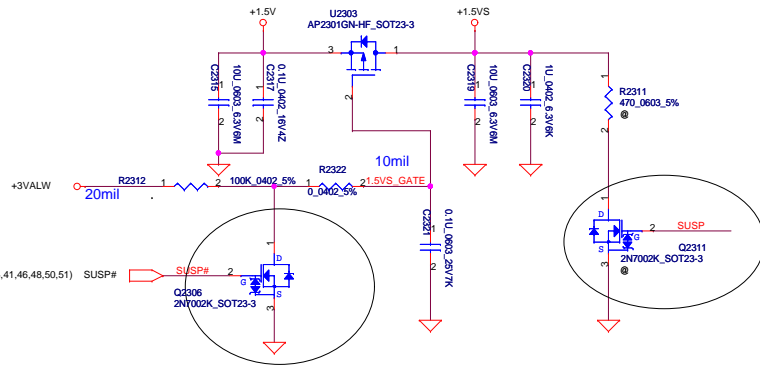


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				Custom	LA-8133P	
				Date:	Friday, January 13, 2012	Sheet 40 of 58

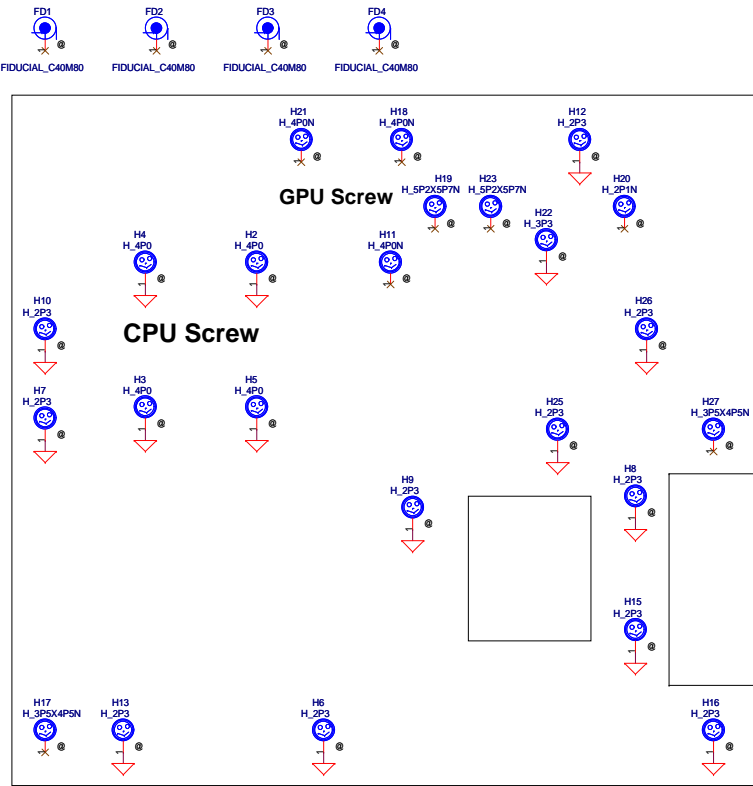


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	EC ENE-KB9012	
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				Custom	LA-8133P	1.0
				Date:	Friday, January 13, 2012	Sheet

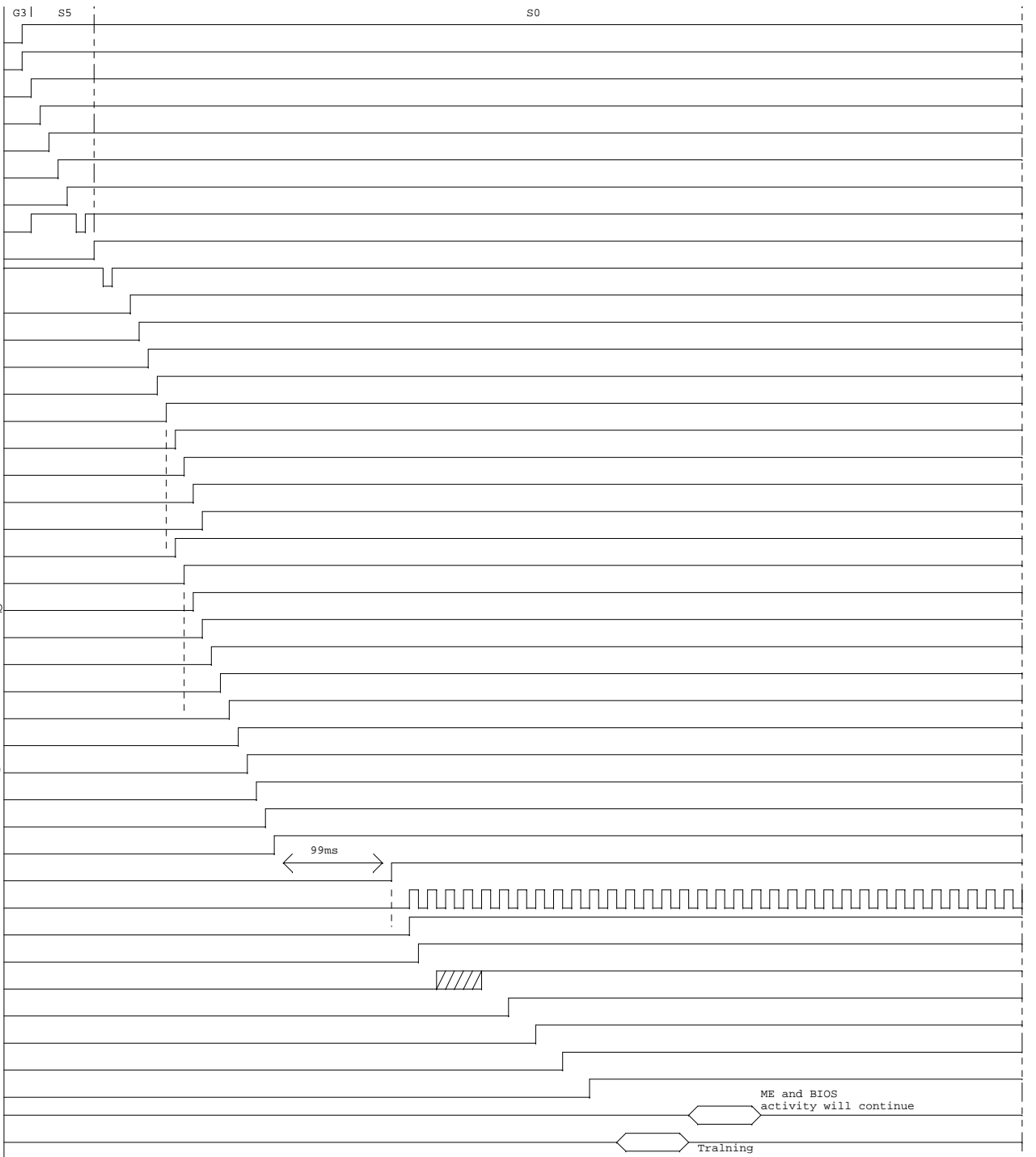
+1.5V to +1.5VS



Screw Hole & FD



- RTC
- RTCRST
- EC_111 pin
- EC_ON
- MAINPWON
- +5VALW
- +3VALW/VCCDSW
- ON/OFF#
- EC_RSMRST#
- PBTN_OUT#
- SLP_S5#
- SLP_S4#
- SYSON
- SYSON
- PCH_SLPA#
- M_PWR_ON
- +3VM
- +1.05VM
- PCH_APWROK
- SLP_S3#
- SUSP#
- +1.5V_CPU_VDDQ
- +1.8VS
- +5VS
- +3VS
- +1.5VS
- +0.75VS
- +V1.05VS (VCCP)
- +VCCSA
- SA_PGOOD
- VR_ON
- PCH_POK
- PCH_CLKOUT
- DRAMPWROK
- H_CPUPWRGD
- CPU_VID
- CPU_CORE
- VGATE
- SYS_PWROK
- BUF_PLT_RST#
- SPI
- DMI

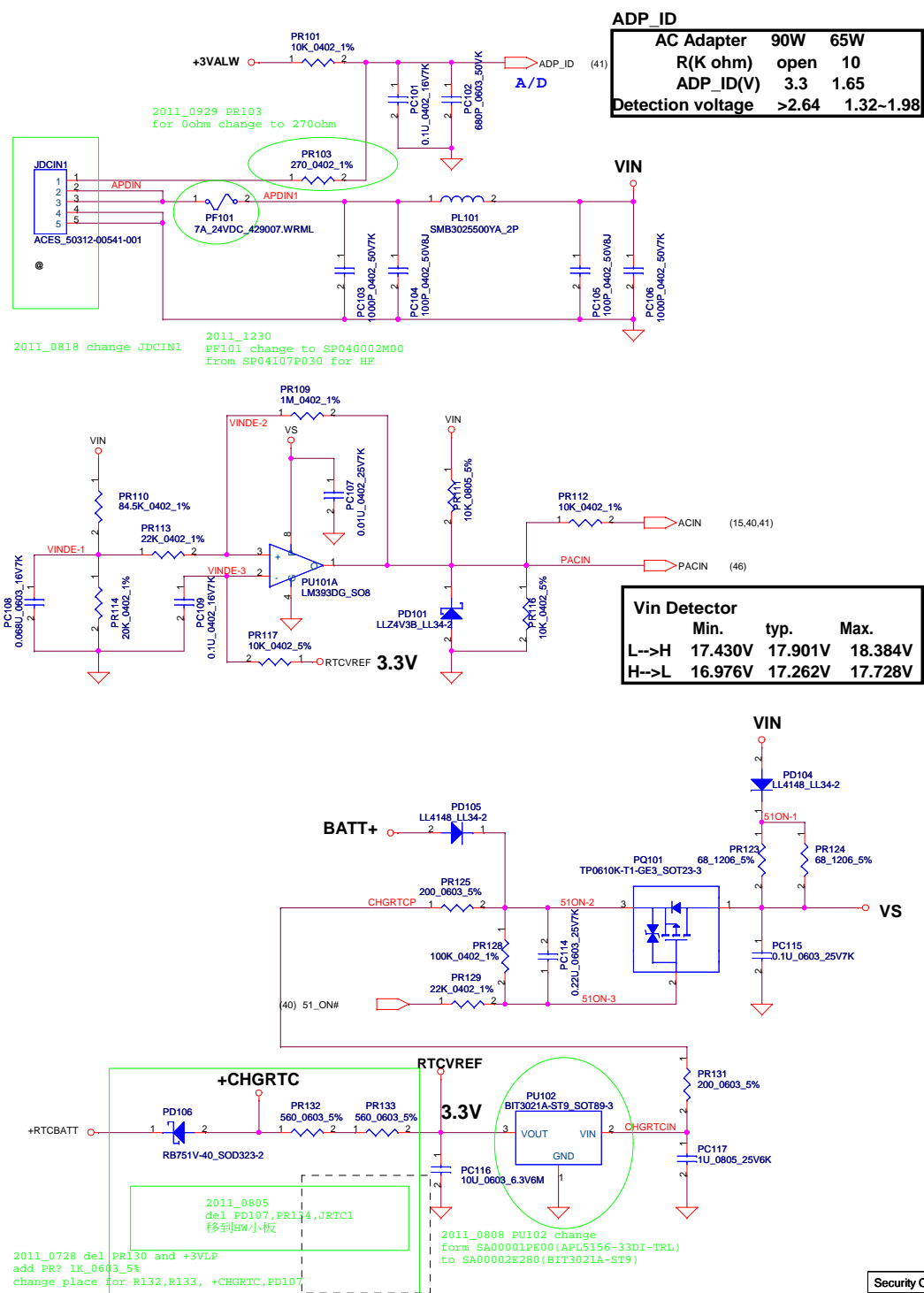


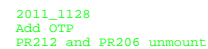
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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Size	Document Number
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Compal Electronics, Inc.

Screw Hole

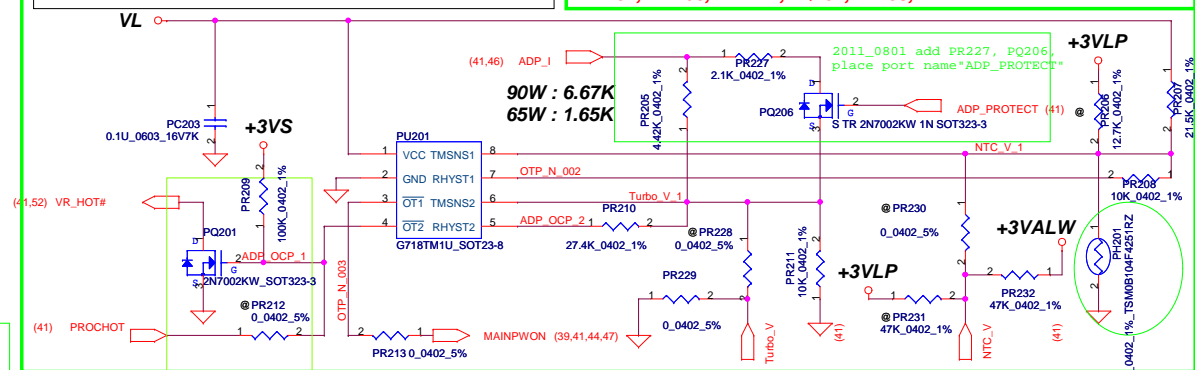
LA-8133P





For KB930 --> Keep PU201 circuit
($V_{th} = 1.25V$)

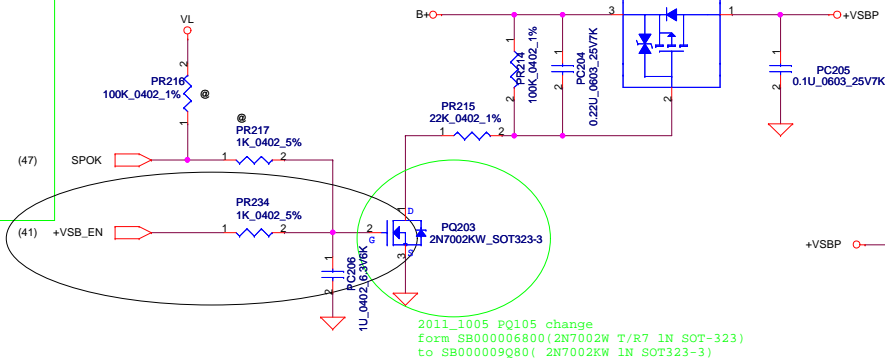
**For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211, PQ201, PR208, PR212**



2011_1119
Change PQ201,PR209,PR212 to mount from unmount

2011_0808
PR227,PQ206
change place

```
2011_1005
PH201 form SL200000V00
100K +-1% NCP15WF104F03RC 0402
change to SL200000U00
100K +-1% TSM0B104F4251RZ 0402
```

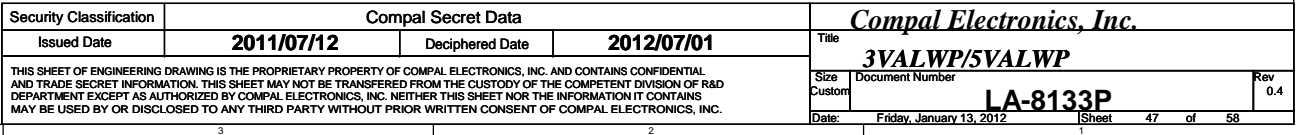


2011_1005 PQ105 change
form SB000006800(2N7002W T/R7 1N SOT-323)
to SB000009Q80(2N7002KW 1N SOT323-3)

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						Size	Document Number			Rev	0.4
						Custom	LA-8133P				
						Date:	Friday, January 13, 2012		Sheet	45	of 58

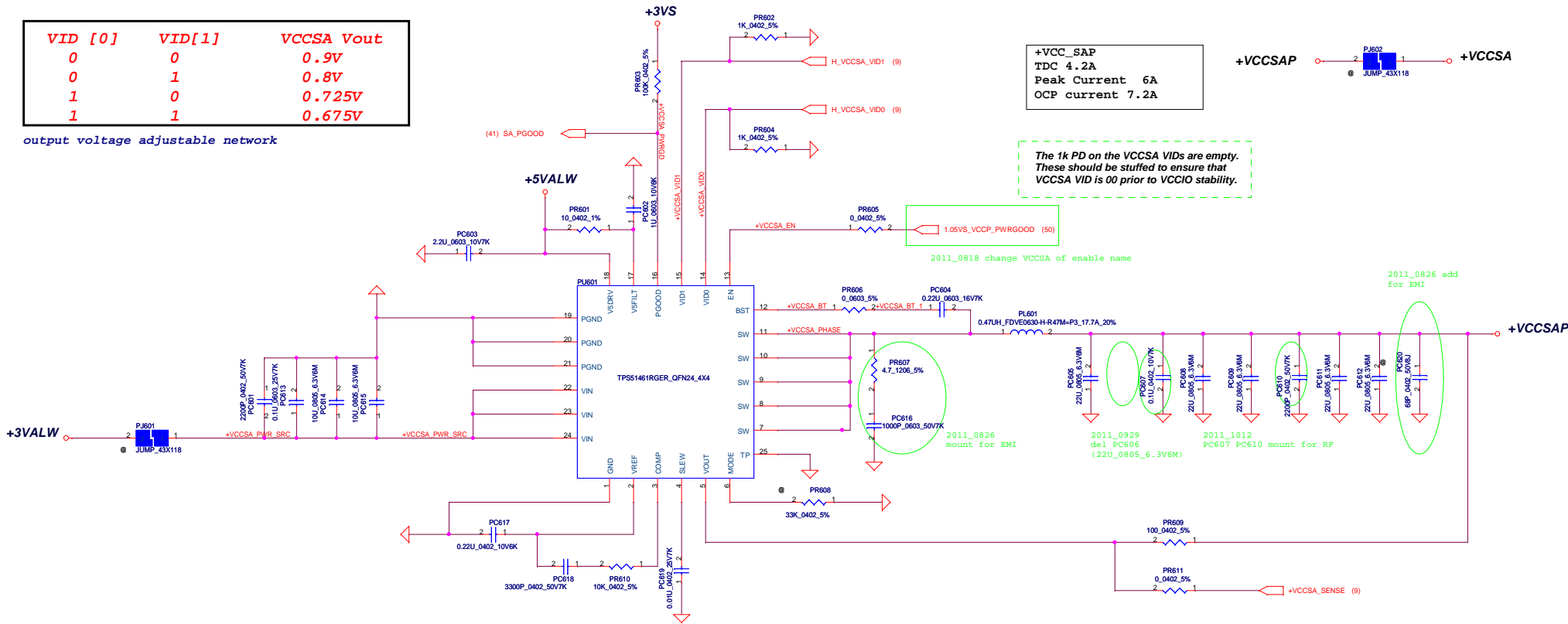
PR415, PR416=>@
add PR415

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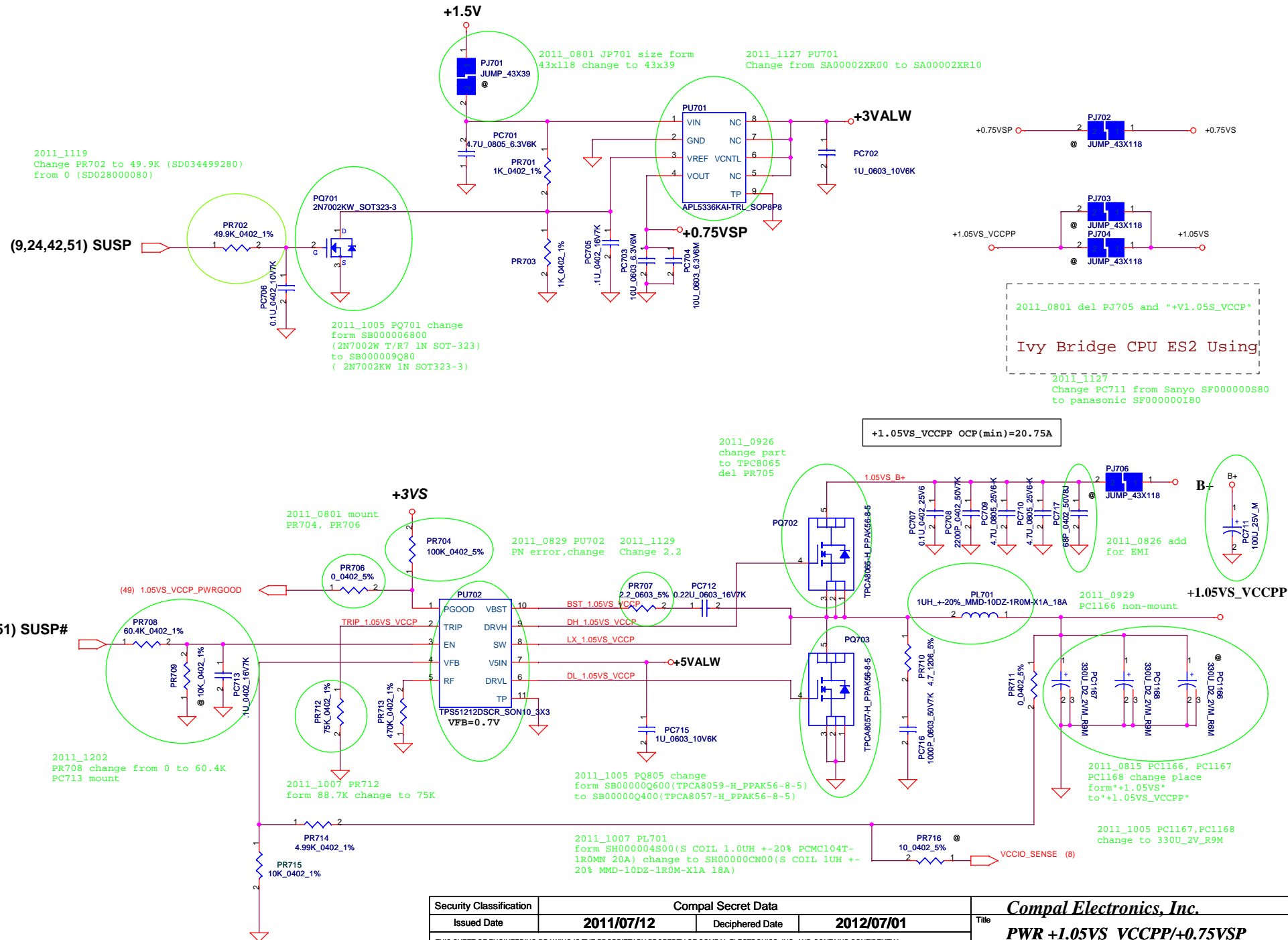


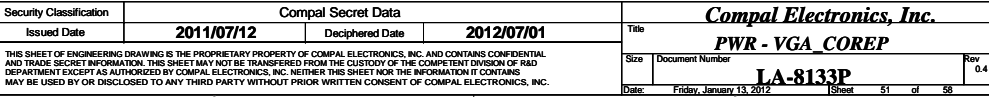
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



2011_0801 del +V1.05S_VCCPP circuit



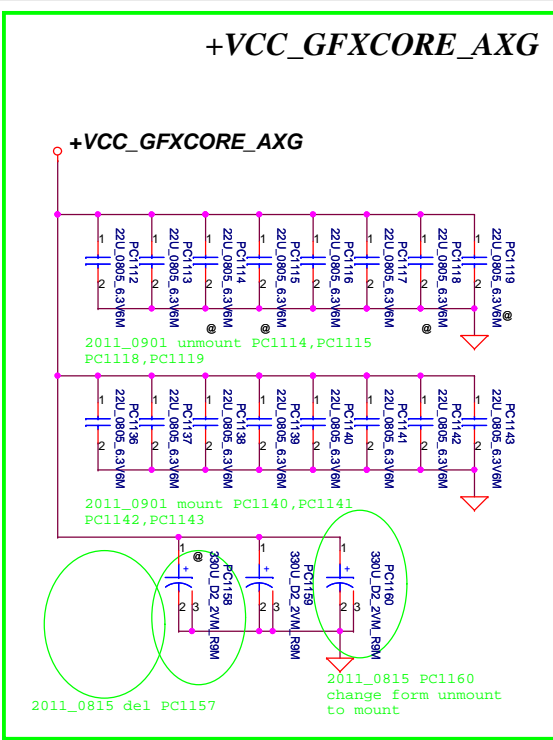
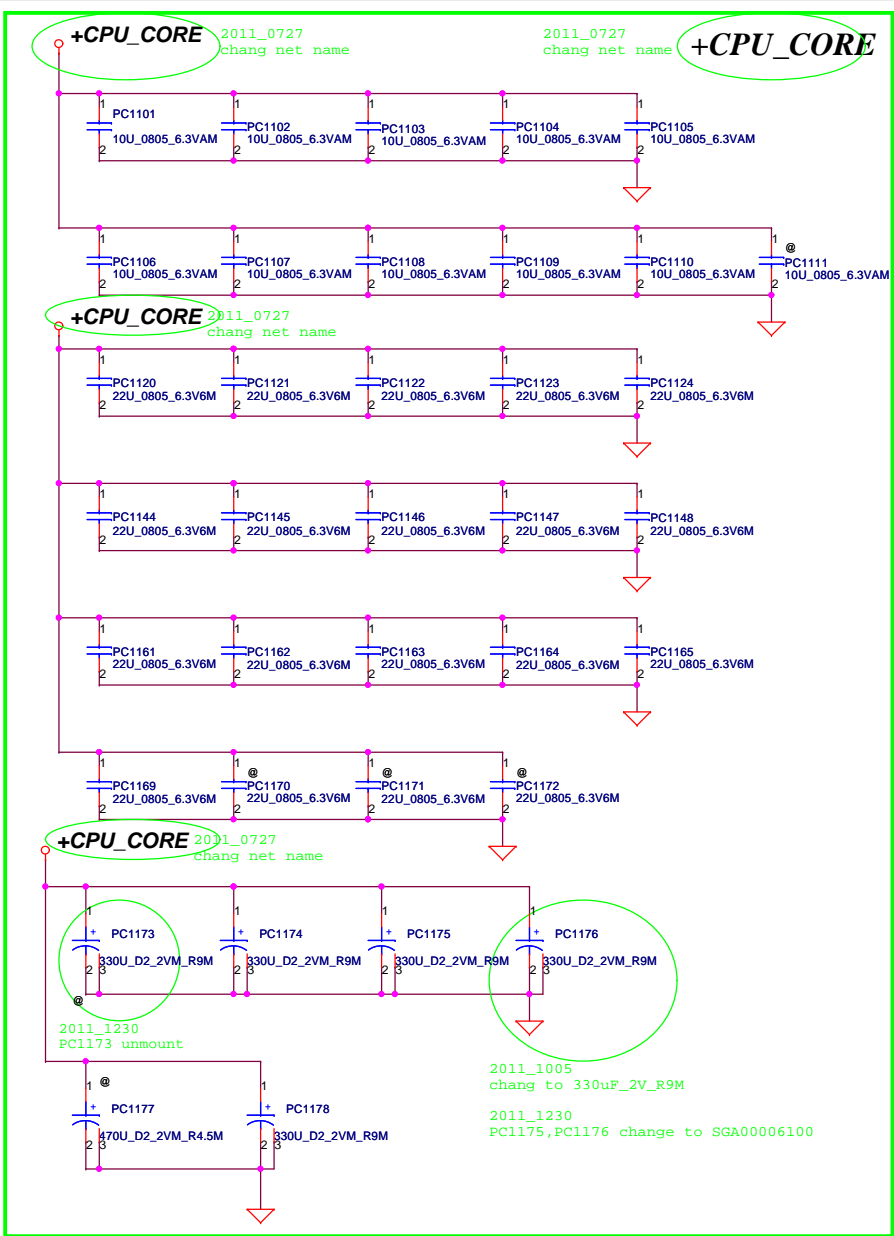


2011_0830
PC901, PC905, PR901, PR903, PR904 mount

2011_1119
Change PC901, PC905 to 0.033u (SE076333K80)
from 0.033u (SE076333KN0)

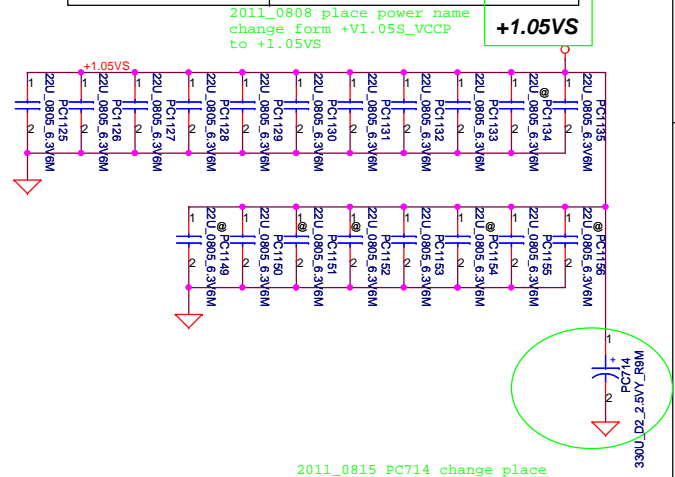
2011_0829
PC909
change part

1. 2011_1007 for function test
2. modify PR903 form 1.21K to 8.2K,
3. PC905 form 4700p to 33n,
4. PR904 form 10.7K to 806,
5. PC907 form 330p to 560p
6. PC909 form 3300p to 1500p
7. PC904 form 330p to 820p
8. PR911 form 63.4K to 66.5K
9. PR942 form 4.32K to 6.04K
10. PC927 form 3300p to 2200p
11. PC934 330p to 820p



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

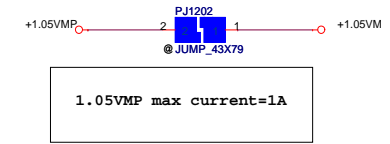
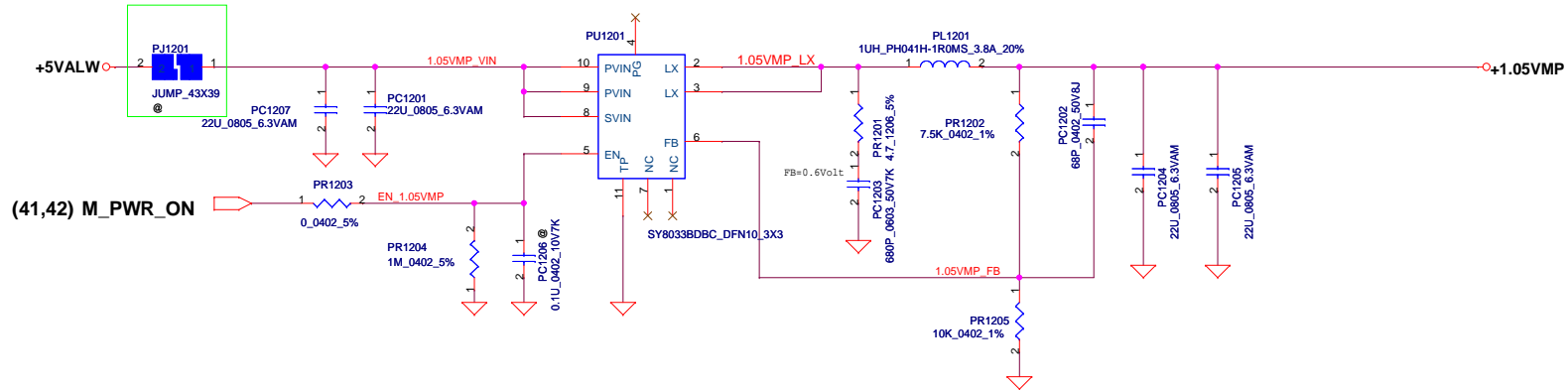


2011_0815 PC714 change place form "+1.05VS_VCCPP" to "+1.05VS"

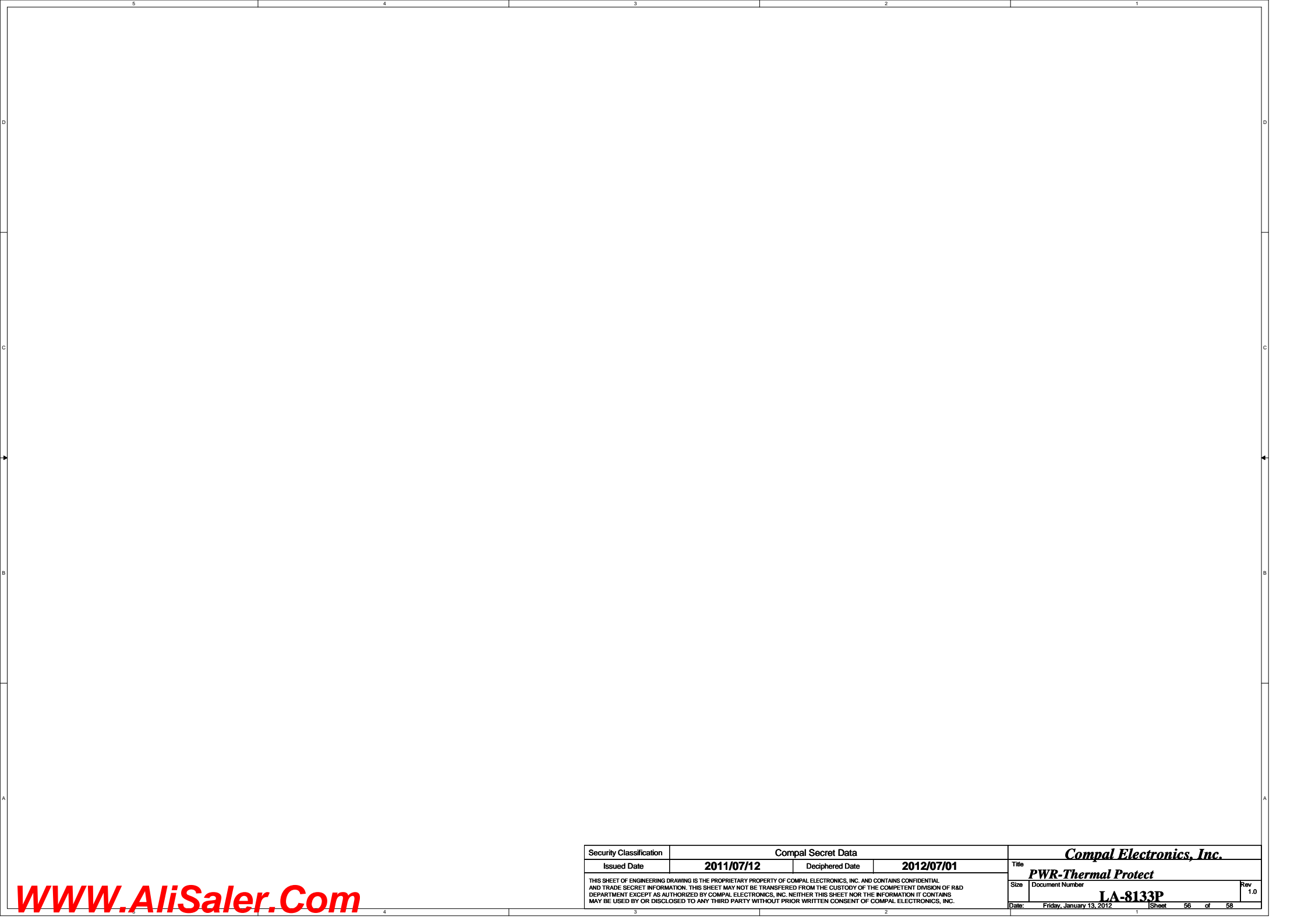
2011_1005 PC714 change to 330uF_2V_R9M

2011_1007 PC714 form SGA00001Q802 (S POLY C 330U 2V M X LESR6M SX H1.9) change to SGA00002680 (330U_D2_2.5VY_R9M)

2011_0923 JUMP form 43X79 change to 43X79



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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function
	2011/09/13	No1		V	V	Add C2325,C2326,C2327,C2328,C2329,R2319,R2324,Q2312	Add SBA function (+3VM) power
	2011/09/15	No2		V		Del Q2305	Del SYSYON#
	2011/09/15	No3		V		Add EC pin 119(M_PWR_ON) for SBA function	Add SBA function
	2011/09/15	No4		V		Add EC pin 120(PCH_SLP#) from PCH to EC for SBA function	Add SBA function
	2011/09/15	No5		V		Add EC pin72 (Muxless_STAT) for GPU STAT	Add Muxless_STAT function
	2011/09/15	No6		V		Del PR310, PR311, PR312, PR313, net name:"H_PROCHOT#", +3VALW.	PWR-CHARGER-BQ24727
	2011/09/15	No7	V			mount PC832	
	2011/09/15	No8		V	V	Add R2482,Q2404,C2509,R2481,R2485,Q2400,R2483,C2501	AOAC Function
	2011/09/15	No9		V	V	change net name BT_OFF# to BT_ON# and change PCH EN GPIO from GPIO34 to GPIO36 R280 from @ to mount,R282 from mount to @	BT Function
	2011/09/15	No10		V	V	change net name(Mini-Express) from BT_OFF# to WLBT_OFF# PCH EN GPIO change to GPIO34	BT Function
	2011/09/19	No11		V	V	change +3VS_WLAN net name to +3VS_AOAC change +3VS_MWAN net name to +3VS_AOAC	AOAC Function
	2011/09/19	No12		V	V	Del R1010 for LVDS CONN plug high voltage	LVDS CONN
	2011/09/19	No13		V	V	R1102,R1104,R1105 from @ to mount fix MIC(ECR97236)issue	MIC function
	2011/09/19	No14		V	V	Add R2470 for 80 port function	80 port function
	2011/09/19	No15		V	V	Del R2476 Add Q2405	BT Function
	2011/09/20	No16		V	V	Add power schematic 9/15 again modify RF PC423, PC425, PC519, PC620, PC717, PC873, PC874, PC124, PC518, PC1017, PC1018, PC1019, PC422, PC516, PC517 modify POWER在VGA的PWM IC 加的零件PR869, PR870	
	2011/09/22	No17		V	V	Add U10,C589,C645 for TPM function	TPM function
	2011/09/22	No18		V	V	Add R110,R112 for SPI POWER choose(SBA function)	
	2011/09/23	No19		V	V	modify power page 44-57(PJ1201 JUMP form 43X79 change to 43X79)	
	2011/09/26	No20		V	V	change CPU footprint from TYCO_2013620-2_989P-T to TYCO_2013620-2_989P-T-A39 change PCH footprint from PANTHER-POINT_FCBGA_989P-T to PANTHER-POINT_FCBGA_989P-T-A39 change GPU footprint N13P-PES-A1_FCBGA_908P to N13P-PES-A1_FCBGA_908P-A39 change VRAM footprint K4W1G1646E-HC12_FBGA_96P to K4W1G1646E-HC12_FBGA_96P-A39	
	2011/09/26	No21		V	V	change PCH_GPIO24(R288) pull up to +3V_PCH	
	2011/09/26	No22		V		change P18 (R311,R330,R286,R329) for UMA and Optimus memon	
	2011/09/26	No23		V		change net name PCH_THRMTRIP#_R to VGA_THRMTRIP#	
	2011/09/26	No24		V	V	PQ702 change to TPC8065,Del PR705 PQ1001,PQ1002,PQ1005 change to TPC8065,Del PR1001,PR1002,PR1007	
	2011/09/26	No25		V	V	p43 change Q2304 dual channel 2n7002 to single channel Q2304,Q2305(Q2305 @) p43 change Q2306 dual channel 2n7002 to single channel Q2306,Q2311(Q2311 @)	
	2011/09/27	No27	V			modify EC Board ID R2213 to 18K	
	2011/09/27	No28		V	V	net name CX_GPIO0 connect to U1101 pin 38	
	2011/09/27	No29		V	V	Add C2152,C2153,D2113 for ESD	
	2011/09/27	No30		V	V	change NVIDIA N13W ROM_SCLK from 15K PU to 5K PU	
	2011/09/27	No31		V	V	change ESD part D2401,D2403,D2405 power from +5VALW to +USB VCCA	
	2011/09/27	No32		V	V	Add C2108 for GPU_CLKREQA	
	2011/09/27	No33				Add Q2406 , modify R2401,Change PCH_GPIO19 to ODD_DET#,for zero power ODD	
	2011/09/27	No34				change WLBT_OFF# to PCH_GPIO34	
	2011/09/27	No35				change PCH_GPIO34 to WLBT_OFF#(mini card pin5)	
	2011/09/27	No36				change BT_ON# connect to WLBT_OFF#(mini card pin51)	
	2011/09/28	No37				C76 , R1123 , c1131 , R2201,C2209 C84,C85 from @ to mount for RF team	
	2011/09/29	No38				R1529 change to 15K	
	2011/09/29	No39				Add CONN JDB3 fo debug	
	2011/09/29	No40				Add R2460,R2438,R2471,R2472,R2475,R2476 for PS8520B	
	2011/09/29	No41				change D2403 ,D2401 power to +USB_VCCB,and del D2403 ,D2401,D2405 Pin3 net	
	2011/09/29	No42				change power schematic del PC606 (22U_0805_6_3V6M) PR855.1 net change form +VGA_CORE to +VGA_COREP PR827 mount change to @(non-mount) PR839 for 47Kohm change to 147Kohm PR103 for 0ohm change to 270ohm PC1166 non-mount,PC1173 non-mount,PC1158 non-mount	
	2011/09/29	No43					
	2011/09/29	No44				Add Q2313,C2305,C2306,C2307,C2308,R2318,R2320,R2320,C2322 for +3V_PCH change CRT CONN to DC061109231(footprint pin modify) Add PR954,PR955	
	2011/09/29	No45				Add H16,H27 change Q2304,Q2305 to Q2304 modify PTH H11,H18 ,H21 Del T10 for SUS_STAT(SLP_S3# 走不出来)	
	2011/10/04	No46				reserve R352,R353 for SATA re-drive PS-8131B change net name from WLBT_OFF to WLBT_OFF_5# modify PCH_GPIO34 connect to BT_ON# for BT module modify PCH_GPIO36 from BT_ON# connect to WLBT_OFF_51# for mini card BT combo module change Q2301 to 2N7002	
	2011/10/05	No47				Del R2469,T49,T45,T41,T37,T36,T28,T26 for ME 限高0 changer power net +3VS_FP to +3VS update power schematics P44-P57	
	2011/10/06	No48				change Q1202 part to SB000007H10. change JCARD1 PN to SP02000H810 footprint: ACES_87213-1400G_14P change some CONN part NO. for ME CONN list Add D2416	

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